1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
02		691395	ENGINEERING RELEASED	04/09/09	?

K36C MLB SCHEMATIC

APR/10/2009

Page (.csa)		Contents		Date
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10	10	CPU FSB	K36B_MLB	08/18/2008
11	11	CPU Power & Ground	K36B_MLB	08/17/2008
12	12	CPU Decoupling	K36B_MLB	08/17/2008
13	13	eXtended Debug Port(MiniXDP)	M99_MLB	01/08/2008
14	14	MCP CPU Interface	K36B_MLB	08/17/2008
15	15	MCP Memory Interface	K36B_MLB	08/17/2008
16	16	MCP Memory Misc	K36B_MLB	08/17/2008
17	17	MCP PCIe Interfaces	K36B_MLB	08/17/2008
18	18	MCP Ethernet & Graphics	K36B_MLB	08/17/2008
19	19	MCP PCI & LPC	K36B_MLB	08/17/2008
20	20	MCP SATA & USB	K36B_MLB	08/17/2008
21	21	MCP HDA & MISC	K36B_MLB	08/17/2008
22	22	MCP Power & Ground	K36B_MLB	08/17/2008
23	24	MCP79 A01 Silicon Support	K36B_MLB	08/17/2008
24	25	MCP Standard Decoupling	K36B_MLB	08/17/2008
25	26	MCP Graphics Support	K36B_MLB	08/17/2008
26	28	SB Misc	K36B_MLB	08/17/2008
27	29	FSB/DDR2 VREF MARGINING	K36B_MLB	08/17/2008
28	31	DDR2 SO-DIMM Connector A	K36B_MLB	08/17/2008
29	32	DDR2 SO-DIMM Connector B	K36B_MLB	08/17/2008
30	33	Memory Active Termination	K36B_MLB	08/17/2008
31	34	Right Clutch Connector	K36B_MLB	08/17/2008
32	37	Ethernet PHY (RTL8211CL)	SUMA	03/20/2008
33	38	Ethernet & AirPort Support	SUMA	04/04/2008
34	39	ETHERNET CONNECTOR	SUMA	04/04/2008
35	41	FireWire LLC/PHY(FW643E)	K36B_MLB	08/17/2008
36	42	FireWire Port Power	K36B_MLB	08/17/2008
37	43	FireWire Ports	K36B_MLB	(MASTER)
38	45	SATA Connectors	K36B_MLB	08/17/2008
39	46	External USB Connectors	K36B_MLB	08/17/2008
40	48	Front Flex Support	K36B_MLB	07/17/2008
41	49	SMC	K36B_MLB	08/17/2008
42	50	SMC Support	K36B_MLB	08/17/2008
43	51	LPC+SPI Debug Connector	K36B_MLB	08/17/2008
44	52	SMBUS CONNECTIONS	K36B_MLB	08/17/2008
45	53	VOLTAGE SENSING	K36B_MLB	08/17/2008
46	54	Current Sensing	K36B_MLB	08/17/2008
47	55	Thermal Sensors	K36B_MLB	08/17/2008
48	56	Fan	K36B_MLB	08/17/2008
49	58	GEYSER	K36B_MLB	08/17/2008
50	59	SMS	K36B_MLB	08/17/2008
51	61	SPI ROM	K36B_MLB	081/17/2008
52	62	AUDIO: CODEC	K36A_MLB	08/29/2008
53	66	AUDI0: SPEAKER AMP	K36A_MLB	08/29/2008
54	67	AUDIO: JACK	K36A_MLB	08/29/2008
55	68	AUDIO: JACK TRANSLATORS	K36A_MLB	08/29/2008
56	69	DC-In & Battery Connectors	RAYMOND	08/17/2008
57	70	PBUS Supply/Battery Charger	K36B_MLB	08/17/2008
58	72	5V/3.3V SUPPLY	K36B_MLB	08/17/2008
59	73	1.8V/0.9V DDR2 SUPPLY	K36B_MLB	08/17/2008
60	74	IMVP6 CPU VCore Regulator	K36B_MLB	08/17/2008
61	75	MCP VCORE REGULATOR	K36B_MLB	08/17/2008
62	76	CPU VTT(1.05V) SUPPLY	K36B_MLB	08/17/2008
63	77	MISC POWER SUPPLIES	K36B_MLB	08/17/2008
64	78	POWER SEQUENCING	K36B_MLB	08/17/2008
65	79	POWER FETS	K36B_MLB	08/17/2008
66	90	INVERTER,LVDS	K36B_MLB	08/17/2008
67	93	TMDS ALIASES	K36B_MLB	08/17/2008
68	94	MINI-DVI CONNECTOR	K36B_MLB	08/17/2008
69	100	CPU/FSB Constraints	K36B_MLB	08/17/2008
70	101	Memory Constraints	K36B_MLB	08/17/2008
71	102	MCP Constraints 1	K36B_MLB	08/17/2008
72	103	MCP Constraints 2	K36B_MLB	08/17/2008
73	104	Ethernet Constraints	K36B_MLB	08/17/2008
74	105	FireWire Constraints	K36B_MLB	08/17/2008
75	106	SMC Constraints	K36B_MLB	08/17/2008
76	109	K36B RULE DEFINITIONS	K36B_MLB	08/17/2008

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8089	1	SCHEM,MLB,K36C	SCH	CRITICAL	
820-2496	1	PCBF,MLB,K36B	PCB	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE: SCHEM,MLB,K36C

DRAWING NUMBER: 051-8089 REV: 02

SHT 1 OF 109

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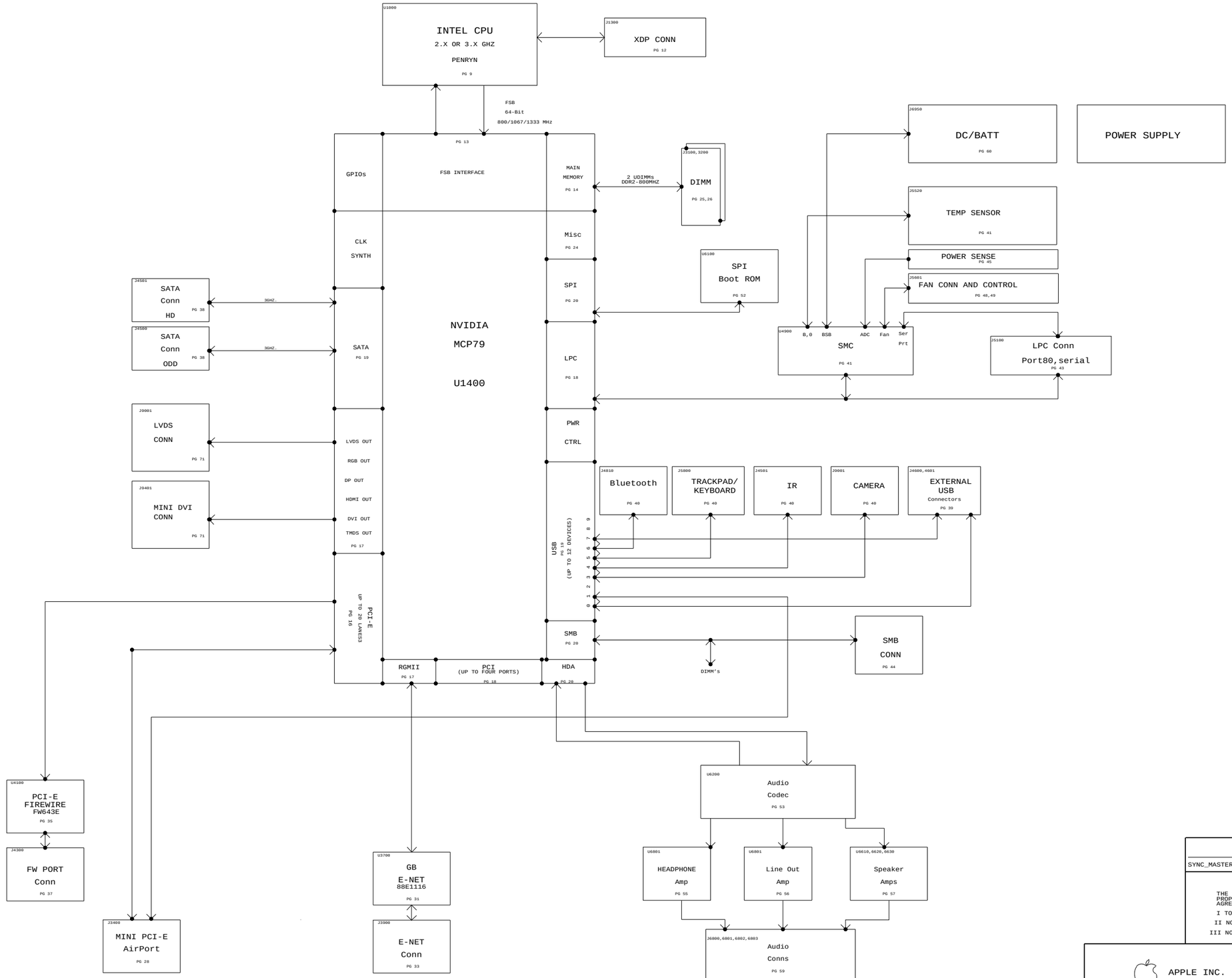

System Block Diagram

SYNC_MASTER=K36B_MLB

SYNC_DATE=08/17/2008

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NONE	2	109

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K36B POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
DCIN(16.5V)
6A FUSE
SMC_DCIN_ISENSE
PBUS SUPPLY/ BATTERY CHARGER
ISL6258A
U7000
CHGR_EN (S5)
ENABLES
VIN
VOUT
U5403
SMC_BATT_ISENSE
D6905
PPVIN_G3H_P3V42G3H
PBUS_VSENSE
Q5315
7A FUSE
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
SHDN*
3.425V G3HOT
LT3470
U6990
PP3V42_G3H_REG
SMC PWRGD
RN5VD30A-F
U5000
SMC_RESET_L
CPUVTTS0_EN (S0)
EN_PSV
CPUVTT
(1.05V)
TPS51117
U7600
PGOOD
CPUVTTS0_PGOOD
PPCPUVTT_S0_REG
(8A MAX CURRENT)
R7955
PP1V05_S0_FET
MCP79
PWRBTN*
LPC_RESET0*
LPC_RESET_L
RSMRST*
CPUPWRGD
CPU_PWRGD
PS_PWRGD
CPU_RESET#
U1400
MCP_PS_PWRGD
U2850
J6950
3S2P
(9 TO 12.6V)
BATT_POS_F
Q7050
CHGR_BGATE
PPVBAT_G3H_CHGR_OUT
CPU VCORE
ISL9504B
IMVP_VR_ON
VR_ON
PGOOD
VR_PWRGOOD_DELAY
SMC_CPU_VSENSE
SMC_CPU_ISENSE
PPVCORE_S0_CPU_REG
(44A MAX CURRENT)
CPU
PWRGOOD
RESET*
U1000
4.6V AUDIO
MAX8902A
U6201
PP4V6_AUDIO_ANALOG
MCP79
PM_SLP_S4_L
SLP_S3#
U1400
PCI_RESET0#
P3V3S3_EN
DDRREG_EN
P5VLTS3_EN
SMC P16
U4900
P60
SMC_PM_G2_EN (S5)
Q7800
RC DELAY
P1V05_S5_EN
1.05V (S5)
TPS62510
U7750
PVIN
PG
P1V05_S5_REG
P1V05_S5_PGOOD
ENTRIP1
ENTRIP2
5V (RT)
3.3V
TPS51125
U7200
PGOOD
VREG3
P5V3V3_PGOOD
PP5VRT_S0_REG
(4A MAX CURRENT)
PP3V3_S5_REG
(4A MAX CURRENT)
PP5VLT_S3_REG
PP3V3_S5
PP3V3_S3_FET
Q7910
Q7930
Q3810
P3V3S3_EN
P3V3S0_EN
P3V3ENET_EN_L
PP3V3_S0_FET
P3V3_ENET_FET
Q3805
PM_SLP_S3_L
PM_WLAN_EN_L
AP_PWR_EN
SMC_ADAPTER_EN
1.5V (S0)
TPS62510
U7740
P1V5S0_EN
PP1V5_S0_FET
P1V5_S0_PGOOD
PP1V8_S0_FET
1.8V S0
FL7700
PP1V8_S0_REG
S3 TO S0 FETS
(Q7901 & Q7971)
R5490
PP1V5_S0
=DDRREG_EN
=DDRVTT_EN
1.8V
0.9V
TPS51116
U7300
PP1V8_S3_REG
(12A MAX CURRENT)
PP0V9_S0_REG
(1A MAX CURRENT)
PM_SLP_S3_L
P1V5S0_EN
MCPDDR_EN
CPUVTTS0_EN
MCPCORES0_EN
P1V05S0_EN (S0)
P3V3S0_EN (S0)
PBUSVSENS_EN (S0)
P5VRTS0_EN_L (S0)
MCP_CORE
5V (LT)
SN0802043
U7500
MCPCORES0_EN
P5VLTS3_EN
PPVCORE_S0_MCP_REG_R
(23A MAX CURRENT)
PP5VLT_S3_REG
(4.5A MAX CURRENT)
PP5V_LT_S3_PGOOD
MCPCORES0_PGOOD
PPVCORE_S0_MCP
PP5VLT_S3
SMC
RSMRST_OUT(P15)
PWRGD(P12)
IMVP_VR_ON(P16)
RSMRST_IN(P13)
SMC_LRESET_L
PWR_BUTTON(P90)
P17(BTN_OUT)
U4900
PM_RSMRST_L
IMVP_VR_ON
PM_PWRBTN_L
SMC_RESET_L
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
P1V5_S0_PGOOD
P5V3V3_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
P5V_LT_S3_PGOOD
S0PGOOD_PWROK
SLP_S5_L
SLP_S4_L
SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
RST*
PP3V3_S0
PP1V8_S0
PP1V05_S0
SEL
ADJ1
ADJ2
LTC2909
U7870

Power Block Diagram

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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D	051-8089	02
SCALE: NONE	SHT 3 OF 109	

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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

BOM OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2420	1	IC,SMC,HSB/2117,9X9MM,TLP,HF,BLANK	U4900	CRITICAL	SMC_PROG
341S2418	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_PROG
341S2093	1	IC, CYPRESS, CY7C63833	U4800	CRITICAL	
338S0654	1	IC,FW643E,1394B PHY/OHCI LINK/PCI-E,127	U4100	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	[EEE:3TN]	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3769	1	PDC,SLGVT,2.26,25W,1066,R0,3M,BGA,P775D	U1000	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0702	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0694	1	IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P	U3700	CRITICAL	

ALTERNATES OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0218		ALL	ALTERNATE PER CYNDI
152S0694	152S0138		ALL	ALTERNATE PER CYNDI
152S0847	152S0586		ALL	ALTERNATE PER CYNDI
152S0874	152S0516		ALL	ALTERNATE PER CYNDI
152S0796	152S0685		ALL	ALTERNATE PER CYNDI
152S0778	152S0693		ALL	ALTERNATE PER CYNDI
157S0058	157S0055		ALL	ALTERNATE PER CYNDI

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0665	1	CONN,RCPT,MINI-DVI,32P,R/A	J9401	CRITICAL	
514-0666	1	CONN,RCPT,3.5MM AUDIO IN,R/A	J6750	CRITICAL	
514-0667	1	CONN,RCPT,3.5MM AUDIO OUT,R/A	J6700	CRITICAL	
514-0668	1	CONN,RCPT,RJ45,NO FILTER,8P	J3900	CRITICAL	
514-0669	1	CONN,RCPT,USB,4P,MIDPLANE	J4600	CRITICAL	
514-0669	1	CONN,RCPT,USB,4P,MIDPLANE	J4601	CRITICAL	

BOARD STACK-UP AND CONSTRUCTION

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

CONFIGURATION OPTIONS

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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D	051-8089	02

SCALE	SHT	OF
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Revision History

*****2008/08/21*****

PAGE 61:
- U7500 PIN V5DRV1 LINK TO PP5V_S0_MCPREG_VCC.
- U7500 PIN TONSEL LINK TO GND DIRECTLY.

PAGE 64:
- R7859 CHANGE TO 100 OHM.
- R7879 CHANGE TO 100K OHM.

PAGE 65:
- DELETE 1.05V S0 FET CIRCUIT.

PAGE 57:
- R7011 CHANGE TO 9.31K OHM, 1%

*****2008/08/22*****

PAGE 7:
- ADD SMC_EXCARD_PWR_EN TEST_POINT

PAGE 8:
- ADD =PP3V42_G3H_RTC_D LINK TO =PP3V42_G3H_REG

PAGE 14:
- R1410 CHANGE TO 49.9 OHM
- CHANGE R1440 TO 150_5% AND NO STUFF

PAGE 26:
- R2872 CHANGE TO 0OHM
- RTC FOLLOW M97 DESIGN AND USE SUPERCAP SOLUTION
- MCP S0 PWRGD FOLLOW M97 DESIGN

PAGE 29:
- PULL R3240 DOWN TO GND. PULL R3241 HIGH

PAGE 32,33,34
- FOLLOW M97 DESIGN

PAGE 39:
- D4600/D4601/PIN-6 CONNECT TO USB VBUS (FOLLOW M97D)

PAGE 44:
- R5270/R5271 = 1K (FOLLOW M97D)
- R5280/R5281 = 1K (FOLLOW M97D)

PAGE 68:
- CHANGE C9411, C9412 TO 220PF
- CHANGE R9462, R9463 TO 2.7KOHM
- ADD C9480 0.1UF_16V_0402 FROM GND_CHASSIS_TMDS_DOWN TO GND
- CHANGE R9460,R9461 TO 0OHM,
- CHANG C9442 AND C9443 TO 47PF

*****2008/08/23*****

MODIFY ALL NOSTUFF TO NO STUFF.

PAGE 6:
- REMOVE ETHERNET CIRCUIT.

PAGE 8:
- ADD =PP3V3_S5_P3V3ENETFET LINK TO PP3V3_S5
- ADD =PP1V05_ENET_PHY LINK TO PP1V2R1V05_ENET.

PAGE 9:
- ADD =RTL8211_ENSWRE LINK TO GND.
- ADD =PP3V3_ENET_PHY_VDDREG LINK TO TP_PP3V3_ENET_PHY_VDDREG.
- ADD =RTL8211_REGOUT LINK TO NC_RTL8211_REGOUT.
- =P3V3ENET_EN_L LINK TO PM_SLP_RMGT_L
- =P1V05ENET_EN LINK TO PM_SLP_RMGT_L

PAGE 10:
- CHANGE XDP_TDO_CONN TO XDP_TDO

PAGE 13:
- XDP FOLLOW M98 DESIGN. CONNECTOR FROM 516S0625 CHANGE TO 998-1571.

PLAGE 23:
- DELETE R2400~R2413 FOR MCP A01 VERSION.

PAGE 31:
- REMOVE R3400, R3401
- L3401 FROM NO STUFF CHANGE TO STUFF.

PAGE 39
- DELETE R4699.
- R4690 FROM NO STUFF CHANGE TO STUFF.

PAGE 41:
- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE
- SMC_NB_CORE_ISENSE CHANGE TO SMC_MCP_CORE_ISENSE

PAGE 46:
- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE
- SMC_NB_CORE_ISENSE CHANGE TO SMC_MCP_CORE_ISENSE
- R5417 ADD BOM OPTION FOR NO STUFF
- R5416 ADD BOM OPTION FOR NO STUFF

PAGE 50:
- ADD C5926 (10UF,20%.0603) TO =PP3V3_S3_SMS

PAGE 63:
- REMOVE USB_PWR_EN_S3

PAGE 66:
- REMOVE R9010, R9011

*****2008/08/24*****

PAGE 6:
- R0602 BOMOPTION FROM JTAG_1DEV CHANGE TO NO STUFF.

PAGE 13:
- XDP FOLLOW M97 DESIGN. CONNECTOR FROM 998-1571 CHANGE TO 516S0625.

PAGE 18:
- R1860 AND R1861 CHANGE TO PAGE 68.

PAGE 25:
- C2504-C2507 FROM 138S0578(402) CHANGE TO 138S0614(402-1)
- C2516-C2517 FROM 138S0578(402) CHANGE TO 138S0614(402-1)

PAG3 35:
- R4150 FROM 118S0343 (0201) CHANGE TO 116S0056(0402)

PAGE 58:
- C7281, C7241, C7272 FROM 138S0555(603) CHANGE TO 138S0615(603-1)
- C7280, C7240 FROM 128S0092(POLY) CHANGE TO 128S0128(POLY-TANT)
- C7291, C7292, C7252, C7251 FROM 128S0115(POLY,CASE-B2) CHANGE TO 128S0222(POLY,CASE-B2-SM)
- Q7260, Q7261 FROM 376S0512 CHANGE TO 376S0652 (H-F)

PAGE 59:
- Q7320 FROM 376S0512 CHANGE TO 376S0652 (H-F)
- Q7321 FROM 376S0511 CHANGE TO 376S0651 (H-F)
- C7321 FROM 128S0111(POLY) CHANGE TO 128S0218 (POLY,CASE-D2E-SM)
- C7343 FROM 128S0073 CHANGE TO 128S0233.

PAGE 60:
- XW7400 ADD BOMOPTION OMIT.
- Q7400, Q7402 FROM 376S0472 CHANGE TO 376S0617.

PAGE 61:
- L7500 FROM 152S0869 CHANGE TO 152S0685.
- Q7500 FROM 376S0512 CHANGE TO 376S0652.
- C7560 FROM 128S0092 CHANGE TO 128S0218.

PAGE 62:
- Q7620 FROM 376S0512 CHANGE TO 376S0652.
- C7601 FROM 138S0578 CHANGE TO 138S0614.

*****2008/08/25*****

CHANGE CSA BASE ON WILL'S SUGGESTION.

PAGE 9:
- ADD GMUX_JTAG_TMS AND GMUX_JTAG_TDI IN MISC NC MCP79 ALIASES.

PAGE 18:
- NETNAME ENET_INTR_L CHANGE TO TP_ENET_INTR_L.
- ENET_PWRDWN_L CHANGE TO TP_ENET_PWRDWN_L

PAGE 19:
- DELETE R1987,R1988,R1995,R1970,R1971,R1972,R1973,R1996,R1997,R1998,R1999,R1978,R1979 (FOLLOW M97 DESIGN).
- NET DPMUX_LOWPWR_L SYNC M97 NETNAME AUD_IPHS_SWITCH_EN
- NET LVDSMUX_SEL_IG_L SYNC M97 NETNAME
- NET DPMUX_SEL_IG_L SYNC M97 NETNAME

PAGE 28:
- REMOVE NET DIMM_OVERTEMPA_L

PAGE 29:
- REMOVE NET DIMM_OVERTEMPA_L

PAGE 42:
- ADD SMC_EXCARD_PWR_EN TO TP_SMC_EXCARD_PWR_EN
- ADD SMC_RSTGATE_L TO TP_SMC_RSTGATE_L
- ADD ALS_GAIN TO NC_ALS_GAIN
- ADD ESTARLDO_EN TO NC_ESTARLDO_EN
- ADD SMC_ANALOG_ID TO NC_SMC_ANALOG_ID
- ADD SMC_SYS_KBDLED TO NC_SMC_SYS_KBDLED
- ADD R5054 10KOHM LINK SMC_GPU_ISENSE PULL DOWN TO GND.
- ADD R5055 10KOHM LINK SMC_NB_MISC_ISENSE PULL DOWN TO GND.

PAGE 43:
- R5142 CHANGE TO NO STUFF.

PAGE 46:
- R5416 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5417 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5418 CHANGE TO 4.53K AND DELETE BOM OPTION.

PAGE 57:
- NETNAME FROM CHGR LOWCURRENT REF CHANGE TO CHGR_LOWCURRENT_REF
- NETNAME FROM CHGR LOWCURRENT GATE CHANGE TO CHGR_LOWCURRENT_GATE

PAGE :
- REMOVE R7884 AND C7884

PAGE 66:
- REMOVE J9001 PIN 20 AND PIN21 NET.

*****2008/09/02*****

PAGE 45:
- CHANGE ODD CONNECTOR FROM 516S0720 TO 516S0719

*****2008/09/27*****

PAGE 9:
- ADD STANDOFF 860-0964 X 4
- ADD STANDOFF 860-0723 X 1
- ADD STANDOFF 860-0749 X 1

PAGE 29:
- REMOVE BOMOPTION TABLE OF R2903/R2905/R2909/R2911

PAGE 66:
- C6601/C6603 CHANGE TO APN 128S0135, and REMOVE BOMOPTION OMIT
- C6605 CHANGE TO APN 128s0148, HF APN 128s0221, and REMOVE BOMOPTION OMIT

PAGE 68:
- C6830/C6831 CHANGE TO APN 128S0220, and REMOVE BOMOPTION OMIT

PAGE 72:
- R7272 CHANGE FROM 57.6K 1%(114s0389) TO 75K 1%(114s0399)

*****2008/10/20*****

PAGE 29:
- ADD R2903/R2905 BOMOTION AND CHANGE VALUE TO 200 OHM

PAGE 50:
- REMOVE ALT TABLE

PAGE 74:
- REMOVE ALT TABLE

PAGE 94:
- REMOVE K36 BOM OPTION TABLE AND ALT TABLE

*****2008/10/22*****

PAGE 12:
- C1200 ~ C1219 CHANGE TO 138S0580

PAGE 28:
- C2870 CHANGE TO 138S0614

PAGE 37:
- ADD R3731 (116s0026 22 ohm 5% 0402) FOR EMI 125MHZ NOISE
- TP_RTL8211_CLK125 CHANGE TO RTL8211_CLK125

PAGE 48:
- C4803 CHANGE TO 138S0614

PAGE 66:
- C6605 CHANGE TO HF APN 128S0221

PAGE 70:
- C7040/C7041/C7047 CHANGE TO 138S0614

PAGE 90:
- L9002 CHANGE TO 116S0004(0ohm,5%,0402)
- C9003 CHANGE TO 116S0004(0ohm,5%,0402)

*****2008/10/24*****

PAGE 19:
- R1950/R1951/R1952/1953 CHANGE TO 116s0004 (0 OHM,5%,0402)

PAGE 28:
- R2825/R2826 CHANGE TO 116s0004 (0 OHM,5%,0402)

PAGE 34:
- J3400 516S0635 CHANGE TO HF APN 516S0729

PAGE 52:
- ADD C5250/C5251/C5270/C5271/C5260/C5261/C5280/C5281 131S1104 (22pF,5%,0402) NO STUFF
- TEXT "ALS" CHANGE TO "MINI-PCIE"
- I2C_ALS_SCL CHANGE TO I2C_MINI_PCIE_SCL
- I2C_ALS_SDA CHANGE TO I2C_MINI_PCIE_SDA

PAGE 67:
- J6700 514-0604 CHANGE TO HF APN 514-0521
- J6750 514-0603 CHANGE TO HF APN 514-0519

PAGE 69:
- J6950 516S0620 CHANGE TO HF APN 516S0735

*****2008/10/25*****

PAGE 52:
- STUFF C5250/C5251/C5270/C5271/C5260/C5261/C5280/C5281

*****2008/10/28*****

PAGE 34:
- J3400 516S0729 CHANGE TO 516S0635

*****2008/10/30*****

PAGE 69:
- J6950 516S0735 CHANGE TO 516S0620

*****2008/10/31*****

PAGE 41:
- U4100 CHANGE FROM 338S0523 TO 338S0654

*****2008/11/01*****

PAGE 4:
- BOM change U1400 CHANGE FROM 338S0678 TO 338S0702

*****2008/11/05*****

PAGE 62:
- C6210 CHANGE FROM 127S0062 TO 127S0108

PAGE 68:
- C6832, C6833 CHANGE FROM 127S0062 TO 127S0108

PAGE 45:
- DELETE L4502, NET SATA_HDD_D2R_UF_P / SATA_HDD_D2R_UF_N
- L4501 / Fl4520 / FL4525 CHANGE FROM 155S0303 TO 155S0371

PAGE 102:
- DELETE PHYSICAL/SPACING SETTING OF SATA_HDD_D2R_UF_P / SATA_HDD_D2R_UF_N

*****2008/11/06*****
- U5413 CHANGE FROM 353S1432 TO 353S2220
- R7417 CHANGE FROM 5.36K(114S0289) TO 4.42K(114S0280)

*****2008/11/12*****
- U1000 CHANGE FROM 373S3646 TO 373S3702

*****2008/11/19*****
- J6950 CHANGE FROM 516S0620 TO 516S0735
- J9401 CHANGE FROM 514-0517 TO 514-0665
- J6750 CHANGE FROM 514-0519 TO 514-0666
- J6700 CHANGE FROM 514-0521 TO 514-0667
- J3900 CHANGE FROM 514-0523 TO 514-0668
- J4600, J4601 CHANGE FROM 514-0527 TO 514-0669
- U3700 CHANGE FROM 338S0570 TO 338S0694

*****2008/11/26*****
- PAGE 61 NOTE : CORRECT REFERENCE TO R5164 AND R5144
- J3400 CHANGE TO 516S0729

*****2008/12/12*****
- R5144 and R5164 changed to 10K 5% 0402 (116S0090)

*****2008/12/17*****
- U4900 symbol update

*****2008/12/20*****
- R5156, R5157, R5158 change from 0 to 33 ohm, 5%, 0402(116s0030)

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

02

SYNC_MASTER=K36B_MLB

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D	051-8089	02

SCALE	SHT	OF
NONE	5	109

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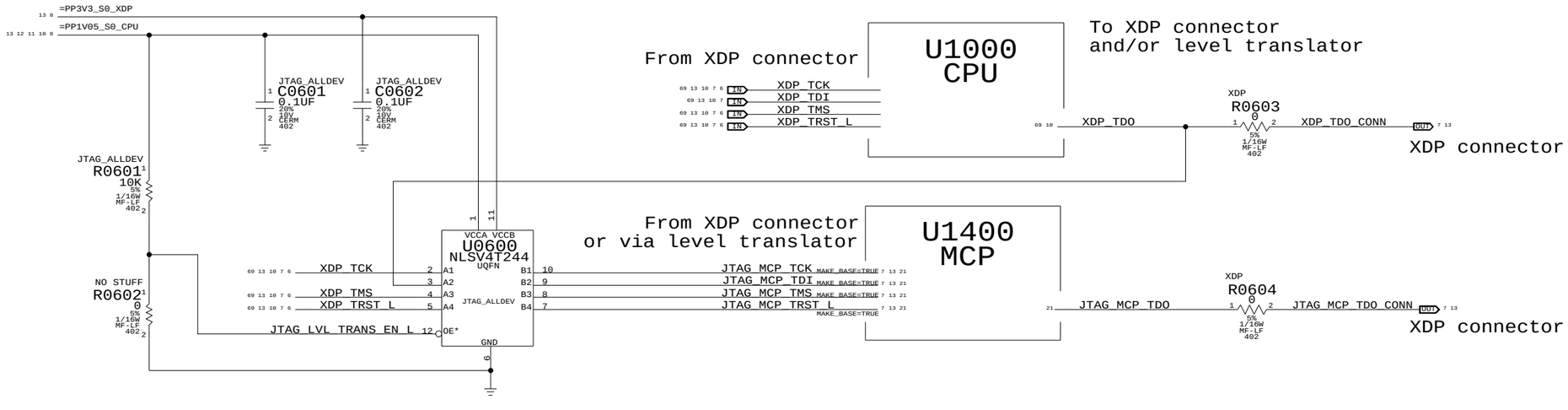
1.05V TO 3.3V LEVEL TRANSLATOR (K36B: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17//2008

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D	051-8089	02

SCALE	SHT	OF
NONE	6	109

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Functional Test Points

#J5601 Fan Connectors

J4100	TRUE	PP5VRT_S0	7 8
J4101	TRUE	FAN_RT_PWM	48
J4102	TRUE	FAN_RT_TACH	48
J4103	TRUE	GND	

#J6950 Battery/Lid Connector

J2801	TRUE	SMC_BS_ALRT_L_F	56
J2802	TRUE	SMBUS_BATT_SCL_F	56
J2803	TRUE	SMBUS_BATT_SDA_F	56
J2804	TRUE	PPVBAT_G3H_CONN_F	56
J2805	TRUE	SMC_LID_F	56
J2901	TRUE	GND_SMC_LID_F	56
J2902	TRUE	PP3V42_G3H_LIDSWITCH_F	56
J2903	TRUE	GND Need 6 TP	

#J6900 MagSafe DC Power Jack

J2401	TRUE	PP18V5_DCIN_FUSE Need 2 TP	56
J2402	TRUE	ADAPTER_SENSE	56
J2403	TRUE	GND Need 2 TP	

#J9000 INVERTER Connector

J2301	TRUE	PPBUS_ALL_INV_CONN Need 2 TP	66
J2302	TRUE	INV_GND	66
J2303	TRUE	PP5V_INV_F	66
J2304	TRUE	INV_BKLIGHT_PWM_L Need 4 TP	66

#J9001 LCD + CAMERA CONNECTOR

J1001	TRUE	PP3V3_LCDVDD_SW_F	66
J1002	TRUE	PP3V3_S0_LCD_F	66
J1003	TRUE	LVDS_IG_DDC_CLK	18 66
J1004	TRUE	LVDS_IG_DDC_DATA	18 66
J1005	TRUE	LVDS_IG_A_DATA_N<0>	18 66 71
J1006	TRUE	LVDS_IG_A_DATA_P<0>	18 66 71
J1007	TRUE	LVDS_IG_A_DATA_N<1>	18 66 71
J1008	TRUE	LVDS_IG_A_DATA_P<1>	18 66 71
J1009	TRUE	LVDS_IG_A_DATA_N<2>	18 66 71
J1010	TRUE	LVDS_IG_A_DATA_P<2>	18 66 71
J1011	TRUE	LVDS_IG_A_CLK_F_N	66
J1012	TRUE	LVDS_IG_A_CLK_F_P	66
J1013	TRUE	USB2_CAMERA_CONN_P	66 72
J1014	TRUE	USB2_CAMERA_CONN_N	66 72
J1015	TRUE	PP5V_S3_CAMERA_F	66
J1016	TRUE	GND	

J6701 MIC CONNECTOR

J1601	TRUE	MIC_LO_CONN	54
J1602	TRUE	MIC_HI_CONN	54
J1603	TRUE	MIC_SHLD_CONN	54 55

#J6702 Left SPEAKER CONNECTOR

J1501	TRUE	SPKRCONN_L_P_OUT	53 54
J1502	TRUE	SPKRCONN_L_N_OUT	53 54

#J6703 Right SUB SPEAKER CONNECTOR

J1503	TRUE	SPKRCONN_SUB_P_OUT	53 54
J1504	TRUE	SPKRCONN_SUB_N_OUT	53 54
J1505	TRUE	SPKRCONN_R_P_OUT	53 54
J1506	TRUE	SPKRCONN_R_N_OUT	53 54

J5800 GEYSER AND DIMM0 REMOTE TEMP SENSORS

J1901	TRUE	TPAD_GND_F	49
J1902	TRUE	CONN_TPAD_ONOFF_FLTR_L	49
J1903	TRUE	CONN_TPAD_USB_P	49 72
J1904	TRUE	CONN_TPAD_USB_N	49 72
J1905	TRUE	SMC_LID_LC	49
J1906	TRUE	PP5V_S3_TPAD_F	49

#J5520 CPU/MCP Thermal Sensor

J1801	TRUE	CPUTHMSNS_D2_P	47
J1802	TRUE	CPUTHMSNS_D2_N	47
J1803	TRUE	MCPTHMSNS_D2_P	47
J1804	TRUE	MCPTHMSNS_D2_N	47

#J4810 BLUETOOTH

J1301	TRUE	PP3V3_S3_BT_F_CONN	40
J1302	TRUE	USB2_BT_F_N_CONN	40 72
J1303	TRUE	USB2_BT_F_P_CONN	40 72
J1304	TRUE	GND_BT_F_CONN	40

#J4500 SATA ODD

J1401	TRUE	SATA_ODD_R2D_UF_P	38 71
J1402	TRUE	SATA_ODD_R2D_UF_N	38 71
J1403	TRUE	SATA_ODD_D2R_C_N	38 71
J1404	TRUE	SATA_ODD_D2R_C_P	38 71
J1405	TRUE	PP3V3_S0 Need 4 TP	7 8
J1406	TRUE	SMC_ODD_DETECT	38 41
J1407	TRUE	GND Need 6 TP	

J4501 SATA HD System LED and IR

J2001	TRUE	SATA_HDD_R2D_P	38 71
J2002	TRUE	SATA_HDD_R2D_N	38 71
J2003	TRUE	SATA_HDD_D2R_C_N	38 71
J2004	TRUE	SATA_HDD_D2R_C_P	38 71
J2005	TRUE	PP5V_S0_HDD_FLT Need 4 TP	38
J2006	TRUE	SYS_LED_ANODE_L	38
J2007	TRUE	IR_RX_OUT	38 40
J2008	TRUE	PP5V_S3_IR_CONN	38
J2009	TRUE	GND Need 4 TP	

#J3400 Airport

J2701	TRUE	PCIE_WAKE_L	17 31
J2702	TRUE	MINI_CLKREQ_L	17 31
J2703	TRUE	PCIE_CLK100M_MINI_N	17 31 71
J2704	TRUE	PCIE_CLK100M_MINI_P	17 31 71
J2705	TRUE	PCIE_MINI_D2R_N	17 31 71
J2706	TRUE	PCIE_MINI_D2R_P	17 31 71
J2707	TRUE	PCIE_MINI_R2D_N	31 71
J2708	TRUE	PCIE_MINI_R2D_P	31 71
J2709	TRUE	PP3V3_WLAN Need 4 TP	31
J2710	TRUE	PP1V5_S0_R Need 3 TP	7 8
J2711	TRUE	MINI_RESET	31
J2712	TRUE	PP3V3_S3_AIRPORT_CONN	31
J2713	TRUE	I2C_MINI_PCIE_SCL	31 44
J2714	TRUE	I2C_MINI_PCIE_SDA	31 44
J2715	TRUE	USB2_AIRPORT_N	31 72
J2716	TRUE	USB2_AIRPORT_P	31 72
J2717	TRUE	GND Need 6 TP	

Other Func Test Points

J2501	TRUE	ALL_SYS_PWRGD	26 41 64
J2502	TRUE	PPVCORE_S0_CPU	8
J2503	TRUE	PPCPUVTT_S0	7 8
J2504	TRUE	PPVCORE_S0_MCP_R	8
J2505	TRUE	PPVCORE_S0_MCP	8
J2506	TRUE	PP0V9_S0	8
J2507	TRUE	PP1V05_S0	7 8
J2508	TRUE	PP1V5_S0_R	7 8
J2509	TRUE	PP1V8_S0	8
J2510	TRUE	PP1V8_S0_R	8
J2511	TRUE	PP1V05_S0_MCP_PEX_AVDD	8 24
J2512	TRUE	PP1V05_S0	7 8
J2513	TRUE	PP1V05_S0_MCP_SATA_AVDD	8 24
J2514	TRUE	PP1V05_S0	7 8
J2515	TRUE	PP5VRT_S0	7 8
J2516	TRUE	PP3V3_S0	7 8
J2517	TRUE	PP1V05_S0_MCP_SATA_AVDD	8 24
J2518	TRUE	PP1V05_S0	7 8
J2519	TRUE	PP5VRT_S0	7 8
J2520	TRUE	PP3V3_S0	7 8
J2521	TRUE	PP1V0_FW	8
J2522	TRUE	PP1V8_S3	8
J2523	TRUE	PP3V3_S3	8
J2524	TRUE	PP5VLT_S3	8
J2525	TRUE	PPVTT_S3_DDR_BUF	8
J2526	TRUE	PP1V05_S5_REG	8
J2527	TRUE	PP3V3_S5	8
J2528	TRUE	PP3V42_G3H	7 8
J2529	TRUE	PP18V5_G3H	8
J2530	TRUE	PPBUS_G3H	8
J2531	TRUE	PPBUS_G3H_CPU_ISNS	8
J2532	TRUE	PP3V3_ENET_PHY	8
J2533	TRUE	PP1V2R1V05_ENET	8
J2534	TRUE	PPVP_FW	8

#J1300 XDP

J1301	TRUE	XDP_BPM_L<5>	10 13 69
J1302	TRUE	XDP_BPM_L<4>	10 13 69
J1303	TRUE	XDP_BPM_L<3>	10 13 69
J1304	TRUE	XDP_BPM_L<2>	10 13 69
J1305	TRUE	XDP_BPM_L<1>	10 13 69
J1306	TRUE	XDP_BPM_L<0>	10 13 69
J1307	TRUE	TP_XDP_OBSFN_B0	13
J1308	TRUE	TP_XDP_OBSFN_B1	13
J1309	TRUE	TP_XDP_OBSDATA_B0	13
J1310	TRUE	TP_XDP_OBSDATA_B1	13
J1311	TRUE	TP_XDP_OBSDATA_B2	13
J1312	TRUE	TP_XDP_OBSDATA_B3	13
J1313	TRUE	XDP_PWRGD	13
J1314	TRUE	XDP_OBS20	13
J1315	TRUE	PM_LATRIGGER_L	13 19
J1316	TRUE	JTAG_MCP_TCK	6 13 21
J1317	TRUE	SMBUS_MCP_0_DATA	13 21 44 72
J1318	TRUE	SMBUS_MCP_0_CLK	13 21 44 72
J1319	TRUE	XDP_TCK	6 10 13 69
J1320	TRUE	PPCPUVTT_S0	7 8
J1321	TRUE	PP3V3_S0	7 8
J1322	TRUE	JTAG_MCP_TDO_CONN	6 13
J1323	TRUE	JTAG_MCP_TRST_L	6 13 21
J1324	TRUE	MCP_DEBUG<0>	13 19 72
J1325	TRUE	MCP_DEBUG<1>	13 19 72
J1326	TRUE	MCP_DEBUG<2>	13 19 72
J1327	TRUE	MCP_DEBUG<3>	13 19 72
J1328	TRUE	JTAG_MCP_TDI	6 13 21
J1329	TRUE	JTAG_MCP_TMS	6 13 21
J1330	TRUE	MCP_DEBUG<4>	13 19 72
J1331	TRUE	MCP_DEBUG<5>	13 19 72
J1332	TRUE	MCP_DEBUG<6>	13 19 72
J1333	TRUE	MCP_DEBUG<7>	13 19 72
J1334	TRUE	FSB_CLK_ITP_P	13 14 69
J1335	TRUE	FSB_CLK_ITP_N	13 14 69
J1336	TRUE	XDP_CPURST_L	13 69
J1337	TRUE	XDP_DBRESET_L	10 13 26
J1338	TRUE	XDP_TDO_CONN	6 13
J1339	TRUE	XDP_TRST_L	6 10 13 69
J1340	TRUE	XDP_TDI	6 10 13 69
J1341	TRUE	XDP_TMS	6 10 13 69
J1342	TRUE	GND Need 8 TP	

J5100 LPC+SPI Connector

J2201	TRUE	PP3V42_G3H	7 8
J2202	TRUE	PP5VRT_S0	7 8
J2203	TRUE	LPC_AD<0>	19 41 43 72
J2204	TRUE	LPC_AD<1>	19 41 43 72
J2205	TRUE	SPI_ALT_MOSI	43
J2206	TRUE	SPI_ALT_MISO	43
J2207	TRUE	LPC_FRAME_L	19 41 43 72
J2208	TRUE	PM_CLKRUN_L	19 41 43
J2209	TRUE	SMC_TMS	41 42 43
J2210	TRUE	DEBUG_RESET_L	26 43
J2211	TRUE	SMC_TDO	41 42 43
J2212	TRUE	SMC_TRST_L	41 43
J2213	TRUE	SMC_MD1	41 43
J2214	TRUE	SMC_TX_L	39 41 42 43
J2215	TRUE	LPC_CLK33M_LPCPLUS	26 43 72
J2216	TRUE	LPC_AD<2>	19 41 43 72
J2217	TRUE	LPC_AD<3>	19 41 43 72
J2218	TRUE	SPIROM_USE_MLB	43
J2219	TRUE	SPI_ALT_CLK	43
J2220	TRUE	SPI_ALT_CS_L	43
J2221	TRUE	LPC_SERIRQ	19 41 43
J2222	TRUE	LPC_PWRDWN_L	19 41 43
J2223	TRUE	SMC_TDI	41 42 43
J2224	TRUE	SMC_TCK	41 42 43
J2225	TRUE	SMC_RESET_L	41 42 43
J2226	TRUE	SMC_NMI	41 43
J2227	TRUE	SMC_RX_L	39 41 42 43
J2228	TRUE	LPCPLUS_GPIO	18 43
J2229	TRUE	GND Need 2 TP	

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FUNC TEST

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SIZE	DRAWING NUMBER	REV.
D	051-8089	02

SCALE	SHT	OF
NONE	7	109

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"S0,S0M" RAILS

=PPVCORE_S0_CPU_REG (CPU VCORE PWR) — PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU
=PPVCORE_S0_CPU_VSENSE

=PPCPUVTT_S0_REG — PPCPUVTT_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU
=PP1V05_S0_MCP_FSB
=PP1V05_S0_SMC_LS

=PPMCPCORE_S0_REG
=PPVCORE_S0_MCP_REG_R (MCP VCORE REG. OUTPUT) — PPVCORE_S0_MCP_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP_VSENSE

=PPVCORE_S0_MCP (MCP VCORE AFTER SENSE RES) — PPVCORE_S0_MCP
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

=PP0V9_S0_REG — PP0V9_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PPVTT_S0_VTTCLAMP
=PP0V9_S3M_MEM_TERM

=PP1V05_S0_FET — PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_AVDD_UF
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_SATA_DVDD
=PP1V05_S0_MCP_HDMI_VDD
=PP1V05_S0_VMON

=PP1V5_S0_FET — PP1V5_S0_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU
=PP1V5_S0_AIRPORT

=PP1V8_S0 (DDR PWR AFTER SENSE RES.) — PP1V8_S0
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8R1V5_S0_MCP_MEM

=PP1V8_S0_FET (DDR PWR REG. OUTPUT) — PP1V8_S0_R
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S0_VMON
=PP1V8_S0_FET_R
=PP3V3R1V8_S0_MCP_IFP_VDD

=PP5VRT_S0_REG — PP5VRT_S0
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_HDD
=PP5V_S0_LPCPLUS
=PP5V_S0_FAN_RT
=PP5V_S0_CPU_IMVP
=PP5V_S0_ODD
=PP5V_S0_TMDS
=PP5V_S0_LCD
=PP5V_S0_CPUVTTS0
=PP5V_S0_AUDIO
=PP5V_S0_AUDIO_AMP

=PP3V3_S0_FET — PP3V3_S0
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP
=PP3V3_S0_MCP
=PP3V3_S0_MCP_DAC_UF
=PP3V3_S0_MCP_VPLL_UF
=PP3V3_S0_ODD
=PP3V3_S0_LPCPLUS
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_SMBUS_MCP_0
=PP3V3_S0_FAN_RT
=PP3V3_S0_AUDIO
=PP3V3_S0_IMVP
=PP3V3_S0_TMDS
=PP3V3_S0_LCD
=PP3V3_S0_MCP_GPIO
=PP3V3_S0_HDCPROM
=PP3V3_S0_MCP_PLL_UF
=PP3V3R1V5_S0_MCP_HDA
=PP3V3_S0_SMC
=PP3V3_S0_MCPTHMSNS
=PP3V3_S0_CPUTHMSNS
=PP5VR3V3_S0_MCPCOREISNS
=PPSPD_S0_MEM
=PP3V3_S0_PWRCTL
=PP3V3_S0_VMON
=PP3V3_S0_MCPDDRISNS
=PP3V3_S0_CPUVTTISNS
=PP3V3_FW_P1V0FW
=PP3V3_FW_PHY
=PP3V3_FW_FWPHY

"S3" RAILS

=PP1V8_S3_REG — PP1V8_S3
MIN_LINE_WIDTH=4.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S3_P1V8S0FET
=PP1V8_S3_MEM

=PP3V3_S3_FET — PP3V3_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_PDCISENS
=PP3V3_S3_SMBUS_SMC_MGMT
=PP3V3_S3_VREFMRGN
=PP3V3_S3_WLAN
=PP3V3_S3_AIRPORT_AUX
=PP3V3_S3_BT
=PP3V3_S3_SMS

=PP5VLT_S3_REG — PP5VLT_S3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_EXTUSB
=PP5V_S3_IR
=PP5V_S3_CAMERA
=PP5V_S3_VTTCLAMP
=PP5V_S3_MCPDDRFET
=PP5V_S3_SYSLED
=PP5V_S3_TPAD
=PP5V_S3_1V8S3_0V9S0
=PP5V_S3_AUDIO
=PP5V_S3_AUDIO_AMP

=PPVTT_S3_DDR_BUF — PPVTT_S3_DDR_BUF
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE

"S5" RAILS

=PP1V05_S5_REG — PP1V05_S5_REG
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S5_MCP_VDD_AUXC
=PP1V05_ENET_P1V05ENETFET

=PP3V3_S5_REG — PP3V3_S5
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO
=PP3V3_S5_ROM
=PP3V3_S5_LCD
=PP3V3_S5_MCP
=PP3V3_S5_MCPPWRGD
=PP3V3_S5_AIRPORT_AUX
=PP3V3_S5_P3V3ENETFET
=PP3V3_S5_PWRCTL
=PP3V3_S5_P1V05ENETFET
=PP3V3_S5_P3V3S3FET
=PP3V3_S5_P3V3S0FET
=PP3V3_S5_P1V05S5
=PP3V3_FW_LATEVG

"FW" RAILS

=PP1V0_FW_REG — PP1V0_FW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.0V
MAKE_BASE=TRUE
=PP1V0_FW_FWPHY

"G3H" RAILS

=PP3V42_G3H_REG — PP3V42_G3H
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=2.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF
=PP3V42_G3H_SMBUS_SMC_BSA
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_CHGR
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_LIDSWITCH
=PP3V42_G3H_BMON_ISNS
=PP3V3_S5_SMC
=PP3V3_S5_LPCPLUS
=PP3V42_G3H_RTC_D

=PP18V5_DCIN_CONN — PP18V5_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PP18V5_G3H_CHGR

=PPBUS_G3H — PPBUS_G3H
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_MCPCORES0
=PPVIN_S0_MCPREG_VIN
=PPVIN_S5_1V8S3_0V9S0
=PPVIN_S5_3V3S5
=PPVIN_S0_5VRTS0
=PPVIN_S3_5VLTS3
=PPBUS_G3HRS5
=PPBUS_S5_INV
=PPBUS_S5_FWPWRSW
=PPBUS_G3H_CPU_ISNS_R

=PPBUS_G3H_CPU_ISNS — PPBUS_G3H_CPU_ISNS
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0
=PPVIN_S5_CPU_IMVP

"ENET" RAILS

=PP3V3_ENET_FET — PP3V3_ENET_PHY
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT
=PP3V3_ENET_PHY

=PP1V05_ENET_FET — PP1V2R1V05_ENET
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_PLL_MAC
=PP1V05_ENET_MCP_RMGT
=PP1V05_ENET_PHY

=PPBUS_S5_FW_FET — PPVP_FW
VOLTAGE=12.6V MIN_NECK_WIDTH=0.2 MM
MAKE_BASE=TRUE MIN_LINK_WIDTH=0.4 MM
=PPVP_FW_PHY_CPS_FET
=PPVP_FW_PORT1

PEX & SATA AVDD/DVDD aliases

PP1V05_S0_MCP_PEX_AVDD (MAKE_BASE=TRUE) — 206 mA (A01)
=PP1V05_S0_MCP_PEX_AVDD0
=PP1V05_S0_MCP_PEX_AVDD1

PP1V05_S0_MCP_PEX_DVDD — 57 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD0
=PP1V05_S0_MCP_PEX_DVDD1

PP1V05_S0_MCP_SATA_AVDD (MAKE_BASE=TRUE) — 127 mA (A01)
=PP1V05_S0_MCP_SATA_AVDD0
=PP1V05_S0_MCP_SATA_AVDD1

=PP1V05_S0_MCP_SATA_DVDD — 43 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD0
=PP1V05_S0_MCP_SATA_DVDD1

Power Aliases

SYNC_MASTER=K36B_MLB

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PCI-E ALIASES

UNUSED GPU LANES

17	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	PEG_PRSNT_L	TP_PEG_PRSNT_L	MAKE_BASE=TRUE
17	PEG_CLKREQ_L	TP_PEG_CLKREQ_L	MAKE_BASE=TRUE
71 17	PEG_CLK100M_P	TP_PEG_CLK100MP	MAKE_BASE=TRUE
71 17	PEG_CLK100M_N	TP_PEG_CLK100MN	MAKE_BASE=TRUE
17	EXTGPU_PWR_EN	TP_EXTGPU_PWR_EN	MAKE_BASE=TRUE
17	EXTGPU_RESET_L	TP_EXTGPU_RESET_L	MAKE_BASE=TRUE

ETHERNET ALIASES

33	=P3V3ENET_EN	PM_SLP_RMGT_L	21, MAKE_BASE=TRUE
33	=P1V05ENET_EN		
32	=PP3V3_ENET_PHY_VDDREG	PP3V3_ENET_PHY_VDDREG	MAKE_BASE=TRUE
32	=RTL8211_REGOUT	NC_RTL8211_REGOUT	MAKE_BASE=TRUE
32	=RTL8211_ENSWREG		

LVDS ALIASES

UNUSED LVDS SIGNALS

71 18	LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P3	NO_TEST=TRUE, MAKE_BASE=TRUE
71 18	LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N3	NO_TEST=TRUE, MAKE_BASE=TRUE
71 18	LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLKP	NO_TEST=TRUE, MAKE_BASE=TRUE
71 18	LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLKN	NO_TEST=TRUE, MAKE_BASE=TRUE
71 18	LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
71 18	LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE

MISC NC MCP79 ALIASES

14	CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE
19	GMUX_JTAG_TDI	TP_GMUX_JTAG_TDI	MAKE_BASE=TRUE
19	GMUX_JTAG_TMS	TP_GMUX_JTAG_TMS	MAKE_BASE=TRUE
16	MCP_MEM_RESET_L	TP_MCP_MEM_RESET_L	MAKE_BASE=TRUE

SO-DIMM ALIASES

UNUSED ADDRESS PINS

28	MEM_A_A<15>	TP_MEM_A_A15	MAKE_BASE=TRUE
29	MEM_B_A<15>	TP_MEM_B_A15	MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

71 17	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2RP	MAKE_BASE=TRUE
71 17	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2RN	MAKE_BASE=TRUE
71 17	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_CP	MAKE_BASE=TRUE
71 17	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_CN	MAKE_BASE=TRUE
17	PCIE_EXCARD_PRSNT_L	TP_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE
17	EXCARD_CLKREQ_L	TP_EXCARD_CLKREQ_L	MAKE_BASE=TRUE
71 17	PCIE_CLK100M_EXCARD_P	TP_PCIE_CLK100M_EXCARDP	MAKE_BASE=TRUE
71 17	PCIE_CLK100M_EXCARD_N	TP_PCIE_CLK100M_EXCARDN	MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

72 20	USB_EXTC_P	TP_USB_EXTCP	MAKE_BASE=TRUE
72 20	USB_EXTC_N	TP_USB_EXTCN	MAKE_BASE=TRUE
72 20	USB_EXTD_P	TP_USB_EXTDP	MAKE_BASE=TRUE
72 20	USB_EXTD_N	TP_USB_EXTDN	MAKE_BASE=TRUE
72 20	USB_EXCARD_P	TP_USB_EXCARDP	MAKE_BASE=TRUE
72 20	USB_EXCARD_N	TP_USB_EXCARDN	MAKE_BASE=TRUE
31	=USB_MINI_P	USB_MINI_P	20 72, MAKE_BASE=TRUE
31	=USB_MINI_N	USB_MINI_N	20 72, MAKE_BASE=TRUE

TRACKPAD(WELLSPRING)

49	=USB2_TPAD_P	USB_TPAD_P	20 72, MAKE_BASE=TRUE
49	=USB2_TPAD_N	USB_TPAD_N	20 72, MAKE_BASE=TRUE

BLUETOOTH

40	=USB2_BT_P	USB_BT_P	20 72, MAKE_BASE=TRUE
40	=USB2_BT_N	USB_BT_N	20 72, MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

69 10	CPU_BSEL<0:2>	=MCP_BSEL<0:2>	14

MAKE_BASE=TRUE; =MCP_BSEL<0:2> OUT

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSV0)

HDA PULL-DOWN

19 AUD_IPHS_SWITCH_EN

R0977 20K 5% 1/16W MF-LF 402

LAN ALIASES

18 MCP_MII_RXER
18 MCP_MII_COL
18 MCP_MII_CRS

R0932 47K 5% 1/16W MF-LF 402
R0931 47K 5% 1/16W MF-LF 402
R0930 47K 5% 1/16W MF-LF 402

DP HOTPLUG PULL-DOWN

18 DP_HOTPLUG_DET

R0940 20K 5% 1/16W MF-LF 402

FW PULL-DOWN

17 PCIE_FW_PRSNT_L

R0955 0 5% 1/16W MF-LF 402

MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

21 MCP_SPKR — R0920 0 5% 1/16W MF-LF 402 — SMC_MCP_SAFE_MODE (IN) 41

MCP_TV_DAC_RSET 18 71
MCP_TV_DAC_VREF 18 71

R0941 124 1% 1/16W MF-LF 402
C0940 0.01UF 10% 16V CERM 402

55 54 53 52 =GND_AUDIO_CODEC — GND_AUDIO_CODEC — XW0901 SM

53 =GND_AUDIO_AMP — GND_AUDIO_AMP — XW0902 SM

MAKE_BASE=TRUE

Screw Holes

BATTERY,AUDIO,DIP DIMM CONNECTOR CHASSIS GND
Z0906 OMIT 5R2P3-7SQBNP

SATA,LVDS CONNECTOR CHASSIS GND
Z0907 OMIT 6P5R2P6-7SQB

DIP DIMM CONNECTOR CHASSIS GND
Z0910 OMIT 5R2P3-7SQB

DIP DIMM CONNECTOR CHASSIS GND
Z0909 OMIT 5R2P3-7SQB

DCIN CONNECTOR CHASSIS GND
Z0902 OMIT 7X7R2P3-5B

I/O CONNECTOR CHASSIS GND
Z0908 OMIT 5P0R2P3-7BLB

56	=GND_BATT_CHGND
54	=GND_CHASSIS_AUDIO_JACK
28	=GND_CHASSIS_DIPDIMM_LEFT
55	=GND_CHASSIS_AUDIO_MIC
66	=GND_CHASSIS_LVDS
29 28	=GND_CHASSIS_DIPDIMM_CENTER
29	=GND_CHASSIS_DIPDIMM_RIGHT
34	=GND_CHASSIS_RJ45
68	=GND_CHASSIS_TMDS_UPPER
37	=GND_CHASSIS_FW_UPPER
68	=GND_CHASSIS_TMDS_DOWN
37	=GND_CHASSIS_FW_DOWN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
860-0964	4	THERMAL STANDOFF	Z0903,Z0904,Z0905,Z0921	?	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0912	?	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES,WIRELESS	Z0913	?	STANDOFF

CPU HEATSINK STANDOFF SCREW HOLE

Z0903 OMIT STDOFF-4.20D3.95H-5.52R3.37-6B

Z0904 OMIT STDOFF-4.20D3.95H-5.52R3.37-7SQB

Z0003 USE SAME Z0913 NON SHAPE OF A HOOF SYMBOL
FOR LAYOUT PLACEMENT
BUT, NEED CHANGE TO HIGH STANDOFF SYMBOL

Z0905 OMIT STDOFF-4.50D3.95H-1.1-3.2-TH

Z0921 OMIT STDOFF-4.50D3.95H-1.1-3.2-TH

Z0901 OMIT 5R2P3-7SQBNP

Z0912 OMIT STDOFF-4.20D2.15H-1.2-3.2-TH

Z0911 OMIT 5R2P3-7B

Z0913 OMIT STDOFF-4.20D3.95H-5.52R3.37-6B

(EMI PAD FOR INVERTER GONNECTOR)

66 INVT_CHGND — ZS0920 EMI-SPRING CLIP-SM-M42

SIGNAL ALIAS

SYNC_MASTER=K36B_MLB

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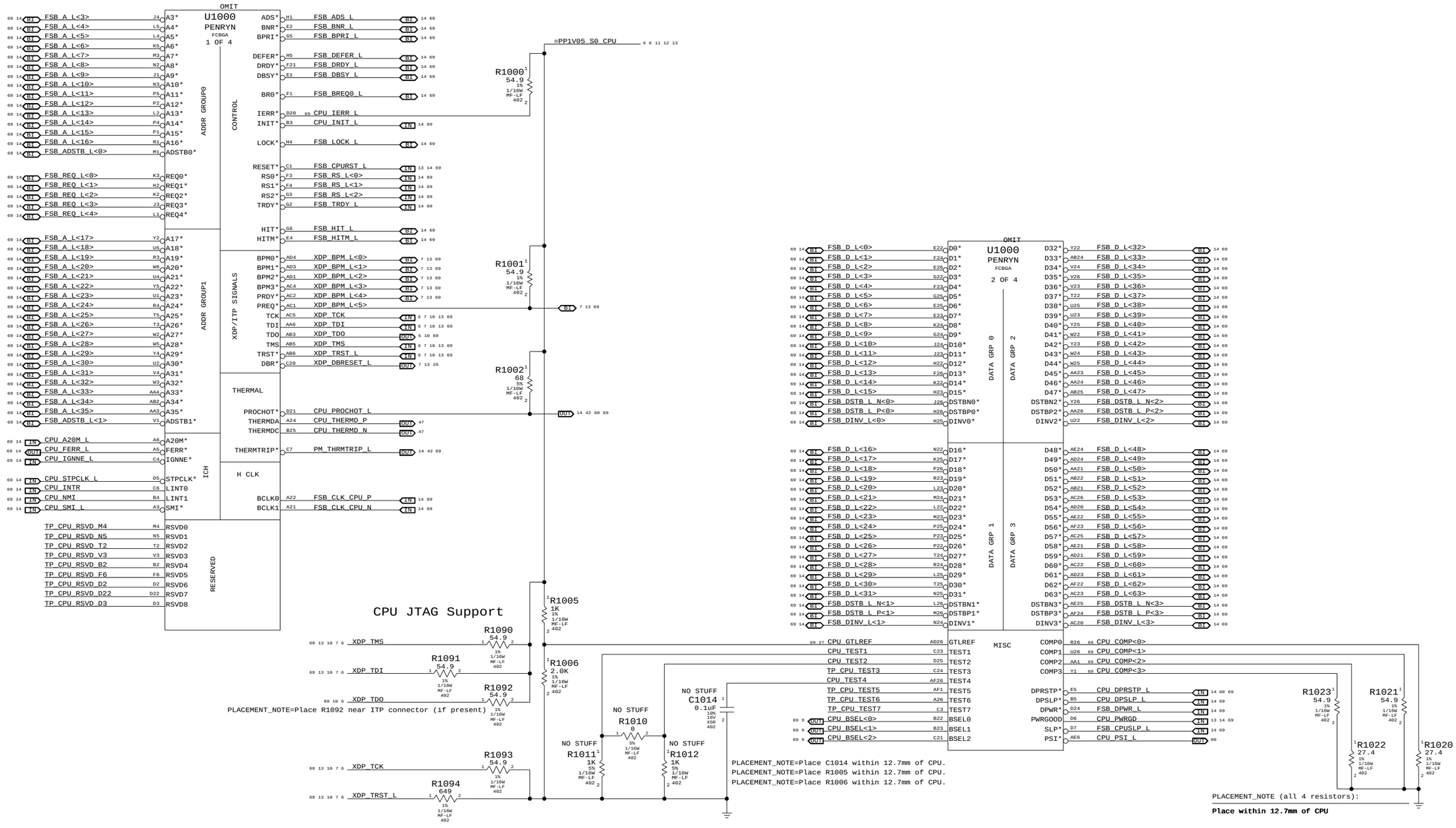

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

CPU FSB

SYNC_MASTER=K36B_MLB SYNC_DATE=08/18/2008

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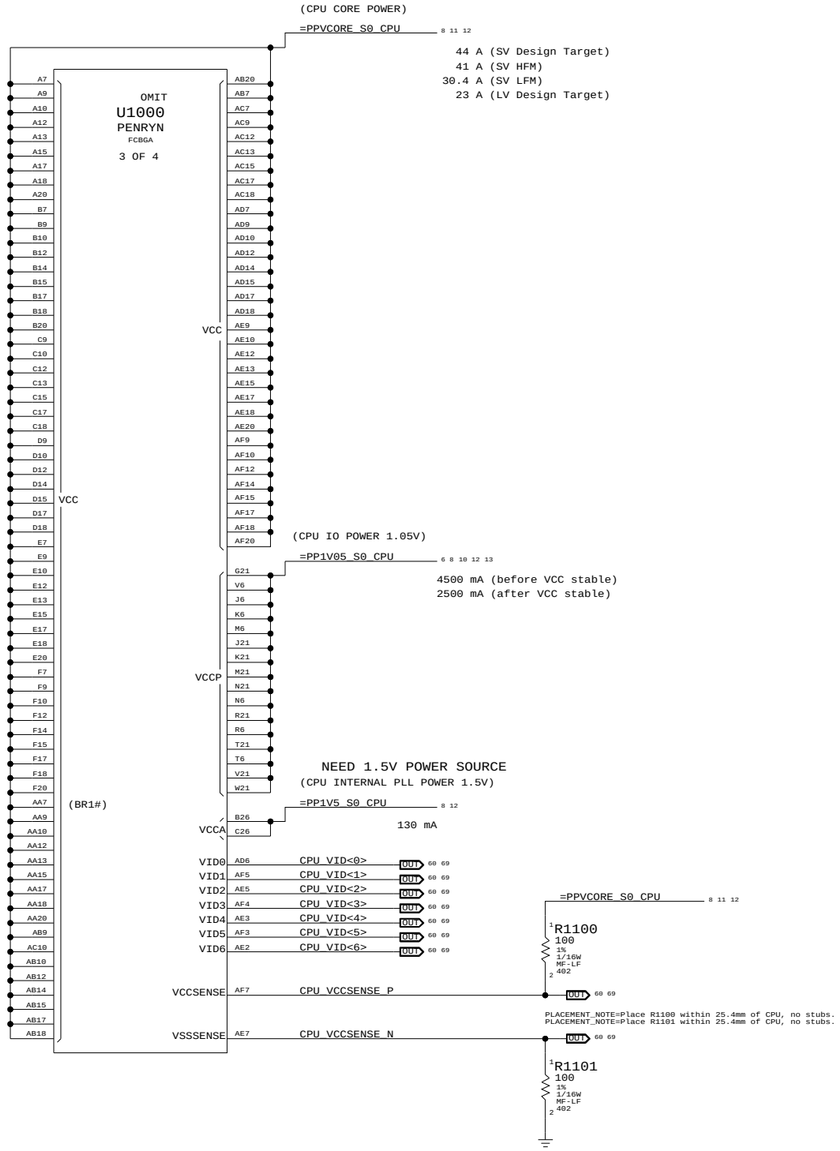

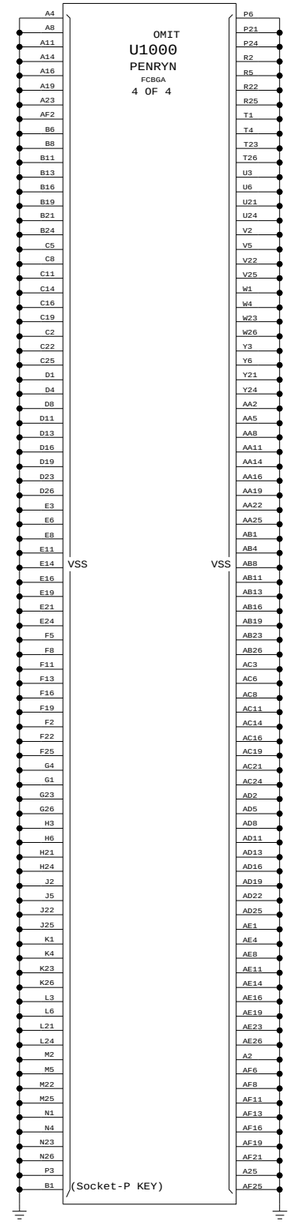

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU Power & Ground

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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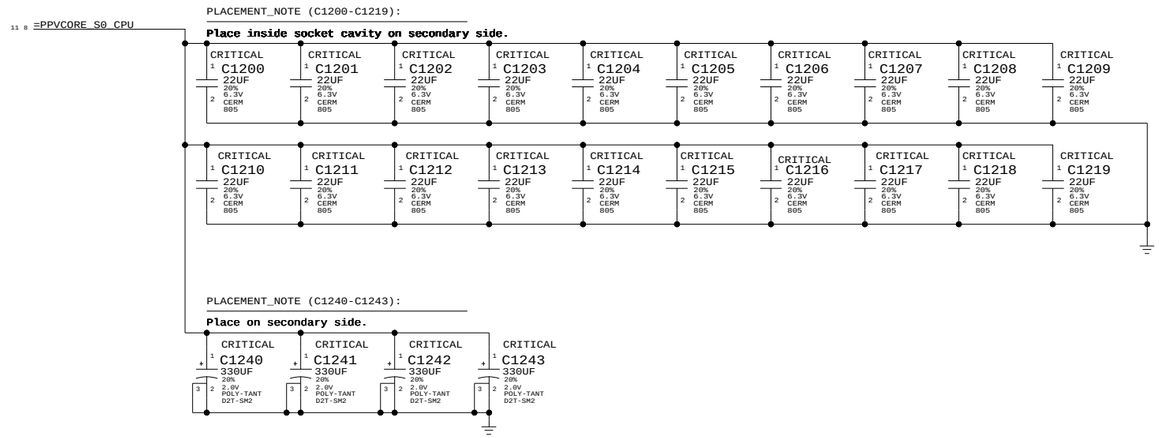
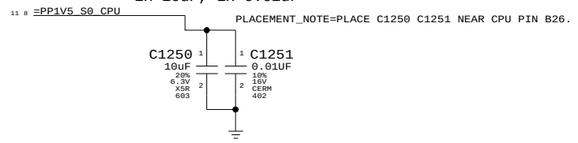
CPU VCore HF and Bulk Decoupling

6x 330uF. 32x 22uF 0805 (20 stuffed)


11 8 =PPVCORE_S0_CPU
PLACEMENT_NOTE (C1200-C1219):
Place inside socket cavity on secondary side.
CRITICAL C1200 22UF 20% 6.3V CERM 805
CRITICAL C1201 22UF 20% 6.3V CERM 805
CRITICAL C1202 22UF 20% 6.3V CERM 805
CRITICAL C1203 22UF 20% 6.3V CERM 805
CRITICAL C1204 22UF 20% 6.3V CERM 805
CRITICAL C1205 22UF 20% 6.3V CERM 805
CRITICAL C1206 22UF 20% 6.3V CERM 805
CRITICAL C1207 22UF 20% 6.3V CERM 805
CRITICAL C1208 22UF 20% 6.3V CERM 805
CRITICAL C1209 22UF 20% 6.3V CERM 805
CRITICAL C1210 22UF 20% 6.3V CERM 805
CRITICAL C1211 22UF 20% 6.3V CERM 805
CRITICAL C1212 22UF 20% 6.3V CERM 805
CRITICAL C1213 22UF 20% 6.3V CERM 805
CRITICAL C1214 22UF 20% 6.3V CERM 805
CRITICAL C1215 22UF 20% 6.3V CERM 805
CRITICAL C1216 22UF 20% 6.3V CERM 805
CRITICAL C1217 22UF 20% 6.3V CERM 805
CRITICAL C1218 22UF 20% 6.3V CERM 805
CRITICAL C1219 22UF 20% 6.3V CERM 805
PLACEMENT_NOTE (C1240-C1243):
Place on secondary side.
CRITICAL C1240 330UF 20% 2.0V POLY-TANT D2T-SM2
CRITICAL C1241 330UF 20% 2.0V POLY-TANT D2T-SM2
CRITICAL C1242 330UF 20% 2.0V POLY-TANT D2T-SM2
CRITICAL C1243 330UF 20% 2.0V POLY-TANT D2T-SM2

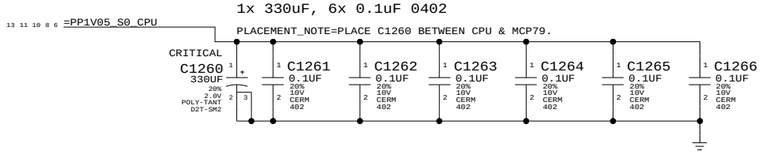
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402


13 11 10 8 6 =PP1V05_S0_CPU
PLACEMENT_NOTE=PLACE C1260 BETWEEN CPU & MCP79.
CRITICAL C1260 330UF 20% 2.0V POLY-TANT D2T-SM2
C1261 0.1UF 20% 10V CERM 402
C1262 0.1UF 20% 10V CERM 402
C1263 0.1UF 20% 10V CERM 402
C1264 0.1UF 20% 10V CERM 402
C1265 0.1UF 20% 10V CERM 402
C1266 0.1UF 20% 10V CERM 402

SYNC FROM T18

CPU Decoupling

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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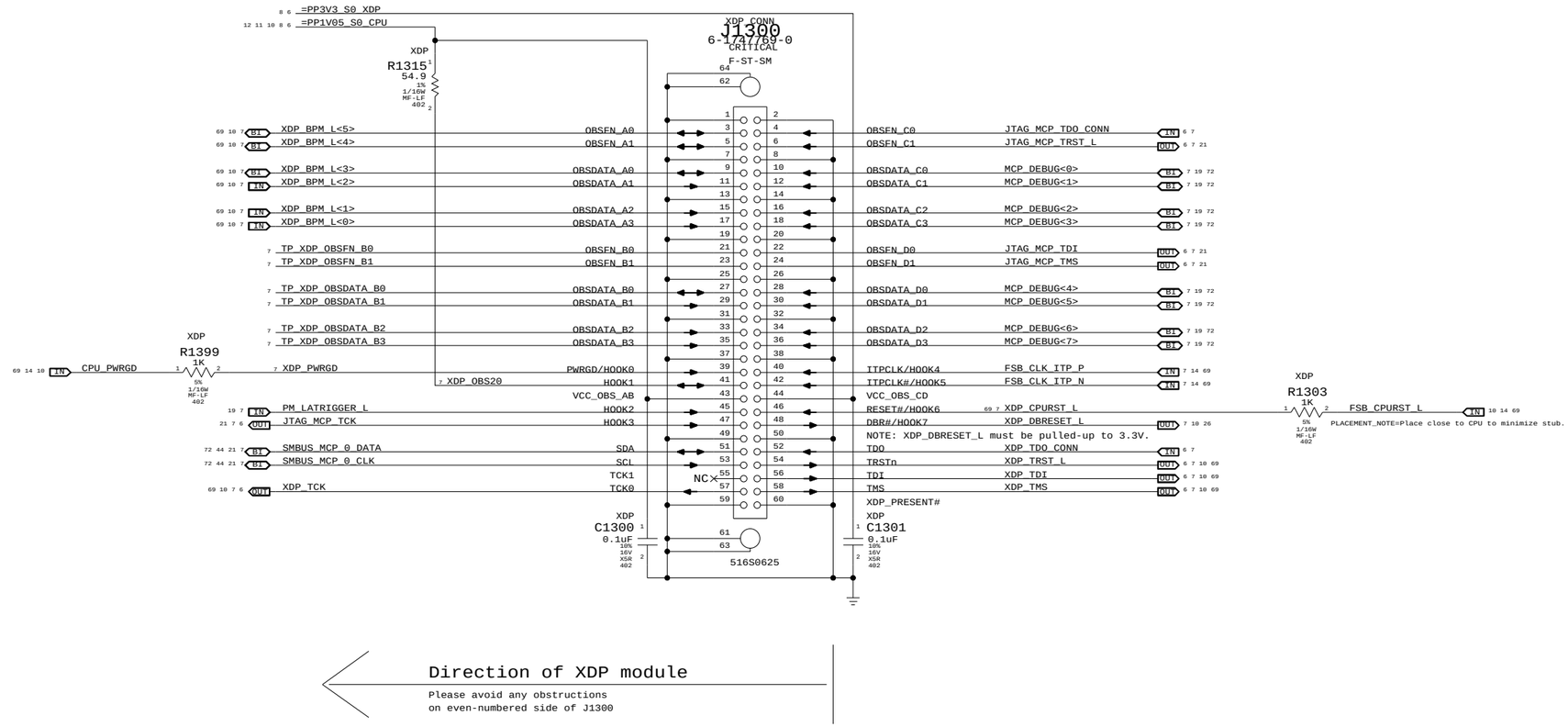
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port(MiniXDP)

SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

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OMIT

U1400

MCP79-TOPO-B

BGA

(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	CPU_D0#	Y43	FSB_D_L<0>		
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	CPU_D1#	W42	FSB_D_L<1>		
FSB_DINV_L<0>	V41	CPU_DBI0#	CPU_D2#	Y40	FSB_D_L<2>		
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	CPU_D3#	W41	FSB_D_L<3>		
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	CPU_D4#	Y39	FSB_D_L<4>		
FSB_DINV_L<1>	V35	CPU_DBI1#	CPU_D5#	V42	FSB_D_L<5>		
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	CPU_D6#	Y41	FSB_D_L<6>		
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	CPU_D7#	Y42	FSB_D_L<7>		
FSB_DINV_L<2>	N35	CPU_DBI2#	CPU_D8#	P42	FSB_D_L<8>		
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	CPU_D9#	U41	FSB_D_L<9>		
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	CPU_D10#	R42	FSB_D_L<10>		
FSB_DINV_L<3>	J41	CPU_DBI3#	CPU_D11#	T39	FSB_D_L<11>		
			CPU_D12#	T42	FSB_D_L<12>		
FSB_A_L<3>	AC34	CPU_A3#	CPU_D13#	T41	FSB_D_L<13>		
FSB_A_L<4>	AE38	CPU_A4#	CPU_D14#	R41	FSB_D_L<14>		
FSB_A_L<5>	AE34	CPU_A5#	CPU_D15#	T43	FSB_D_L<15>		
FSB_A_L<6>	AC37	CPU_A6#	CPU_D16#	W35	FSB_D_L<16>		
FSB_A_L<7>	AE37	CPU_A7#	CPU_D17#	AA37	FSB_D_L<17>		
FSB_A_L<8>	AE35	CPU_A8#	CPU_D18#	W33	FSB_D_L<18>		
FSB_A_L<9>	AB35	CPU_A9#	CPU_D19#	W34	FSB_D_L<19>		
FSB_A_L<10>	AF35	CPU_A10#	CPU_D20#	AA36	FSB_D_L<20>		
FSB_A_L<11>	AG35	CPU_A11#	CPU_D21#	AA34	FSB_D_L<21>		
FSB_A_L<12>	AG39	CPU_A12#	CPU_D22#	AA38	FSB_D_L<22>		
FSB_A_L<13>	AE33	CPU_A13#	CPU_D23#	AA35	FSB_D_L<23>		
FSB_A_L<14>	AG37	CPU_A14#	CPU_D24#	U38	FSB_D_L<24>		
FSB_A_L<15>	AG38	CPU_A15#	CPU_D25#	U36	FSB_D_L<25>		
FSB_A_L<16>	AG34	CPU_A16#	CPU_D26#	U35	FSB_D_L<26>		
FSB_A_L<17>	AN38	CPU_A17#	CPU_D27#	U33	FSB_D_L<27>		
FSB_A_L<18>	AL39	CPU_A18#	CPU_D28#	U34	FSB_D_L<28>		
FSB_A_L<19>	AG33	CPU_A19#	CPU_D29#	W38	FSB_D_L<29>		
FSB_A_L<20>	AL33	CPU_A20#	CPU_D30#	R33	FSB_D_L<30>		
FSB_A_L<21>	AJ33	CPU_A21#	CPU_D31#	U37	FSB_D_L<31>		
FSB_A_L<22>	AN36	CPU_A22#	CPU_D32#	N34	FSB_D_L<32>		
FSB_A_L<23>	AJ35	CPU_A23#	CPU_D33#	N33	FSB_D_L<33>		
FSB_A_L<24>	AJ37	CPU_A24#	CPU_D34#	R34	FSB_D_L<34>		
FSB_A_L<25>	AJ36	CPU_A25#	CPU_D35#	R35	FSB_D_L<35>		
FSB_A_L<26>	AJ38	CPU_A26#	CPU_D36#	P35	FSB_D_L<36>		
FSB_A_L<27>	AL37	CPU_A27#	CPU_D37#	R39	FSB_D_L<37>		
FSB_A_L<28>	AL34	CPU_A28#	CPU_D38#	R37	FSB_D_L<38>		
FSB_A_L<29>	AN37	CPU_A29#	CPU_D39#	R38	FSB_D_L<39>		
FSB_A_L<30>	AJ34	CPU_A30#	CPU_D40#	L37	FSB_D_L<40>		
FSB_A_L<31>	AL38	CPU_A31#	CPU_D41#	L39	FSB_D_L<41>		
FSB_A_L<32>	AL35	CPU_A32#	CPU_D42#	L38	FSB_D_L<42>		
FSB_A_L<33>	AN34	CPU_A33#	CPU_D43#	N36	FSB_D_L<43>		
FSB_A_L<34>	AR39	CPU_A34#	CPU_D44#	N38	FSB_D_L<44>		
FSB_A_L<35>	AN35	CPU_A35#	CPU_D45#	J39	FSB_D_L<45>		
			CPU_D46#	J38	FSB_D_L<46>		
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	CPU_D47#	J37	FSB_D_L<47>		
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	CPU_D48#	L42	FSB_D_L<48>		
			CPU_D49#	M42	FSB_D_L<49>		
FSB_REQ_L<0>	AC38	CPU_REQ0#	CPU_D50#	P41	FSB_D_L<50>		
FSB_REQ_L<1>	AA33	CPU_REQ1#	CPU_D51#	N41	FSB_D_L<51>		
FSB_REQ_L<2>	AC39	CPU_REQ2#	CPU_D52#	N40	FSB_D_L<52>		
FSB_REQ_L<3>	AC33	CPU_REQ3#	CPU_D53#	M40	FSB_D_L<53>		
FSB_REQ_L<4>	AC35	CPU_REQ4#	CPU_D54#	H40	FSB_D_L<54>		
			CPU_D55#	K42	FSB_D_L<55>		
FSB_ADS_L	AD42	CPU_ADS#	CPU_D56#	H41	FSB_D_L<56>		
FSB_BNR_L	AD43	CPU_BNR#	CPU_D57#	L41	FSB_D_L<57>		
FSB_BREQ0_L	AE40	CPU_BR0#	CPU_D58#	H43	FSB_D_L<58>		
FSB_BREQ1_L	AL32	CPU_BR1#	CPU_D59#	H42	FSB_D_L<59>		
FSB_DBSY_L	AD39	CPU_DBSY#	CPU_D60#	K41	FSB_D_L<60>		
FSB_DRDY_L	AD41	CPU_DRDY#	CPU_D61#	J40	FSB_D_L<61>		
FSB_HIT_L	AB42	CPU_HIT#	CPU_D62#	H39	FSB_D_L<62>		
FSB_HITM_L	AD40	CPU_HITM#	CPU_D63#	M43	FSB_D_L<63>		
FSB_LOCK_L	AC43	CPU_LOCK#					
FSB_TRDY_L	AE41	CPU_TRDY#	CPU_BPRI#	AA41	FSB_BPRI_L		
			CPU_DEFER#	AA40	FSB_DEFER_L		
CPU_PECI_MCP	E41	CPU_PECI					
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P		
	AG43	CPU_THERMTRIP#	BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N		
	AH40	CPU_FERR#					
			BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P		
(MCP_BSEL<2>)	F42	CPU_BSEL2	BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N		
(MCP_BSEL<1>)	D42	CPU_BSEL1					
(MCP_BSEL<0>)	F41	CPU_BSEL0	BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P		
			BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N		
FSB_RS_L<0>	AC41	CPU_RS0#					
FSB_RS_L<1>	AB41	CPU_RS1#	BCLK_IN_N	AK41			
FSB_RS_L<2>	AC42	CPU_RS2#	BCLK_IN_P	AJ40			
PP1V05_S0_MCP_PLL_FSB							
270 mA (A01)	206 mA	AG27 +V_DLL_DLCELL_AVDD					
	20 mA	AH27 +V_PLL_MCLK					
	29 mA	AG28 +V_PLL_FSB					
	15 mA	AH28 +V_PLL_CPU					
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	CPU_A20M#	AF41	CPU_A20M_L		
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	CPU_IGNNE#	AH39	CPU_IGNNE_L		
			CPU_INIT#	AH42	CPU_INIT_L		
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	CPU_INTR	AF42	CPU_INTR		
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	CPU_NMI	AG41	CPU_NMI		
			CPU_SMI#	AH41	CPU_SMI_L		
			CPU_PWRGD	AH43	CPU_PWRGD		
			CPU_RESET#	H38	FSB_CPURST_L		
			CPU_SLP#	AM33	FSB_CPUSLP_L		
			CPU_DPSLP#	AN33	CPU_DPSLP_L		
			CPU_DPWR#	AM32	FSB_DPWR_L		
			CPU_STPCLK#	AG42	CPU_STPCLK_L		
			CPU_DPRSTP#	AN32	CPU_DPRSTP_L		

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402

R1415 62 5% 1/16W MF-LF 402

R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L

CPU_FERR_L

NO STUFF R1420 1K 5% 1/16W MF-LF 402

NO STUFF R1421 1K 5% 1/16W MF-LF 402

NO STUFF R1422 1K 5% 1/16W MF-LF 402

=MCP_BSEL<2>

=MCP_BSEL<1>

=MCP_BSEL<0>

R1430 49.9 1% 1/16W MF-LF 402

R1435 49.9 1% 1/16W MF-LF 402

R1431 49.9 1% 1/16W MF-LF 402

R1436 49.9 1% 1/16W MF-LF 402

=PP1V05_S0_MCP_FSB

NO STUFF

R1440 150 5% 1/16W MF-LF 402

MCP CPU Interface

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SYNC_DATE=08/17/2008

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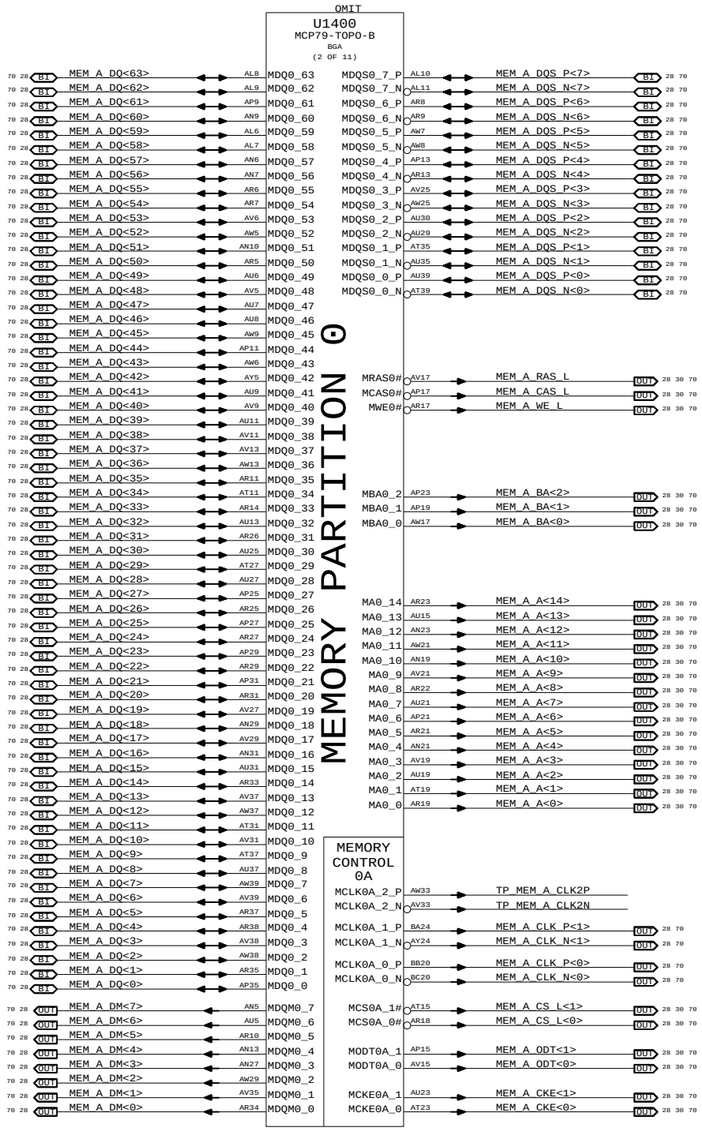

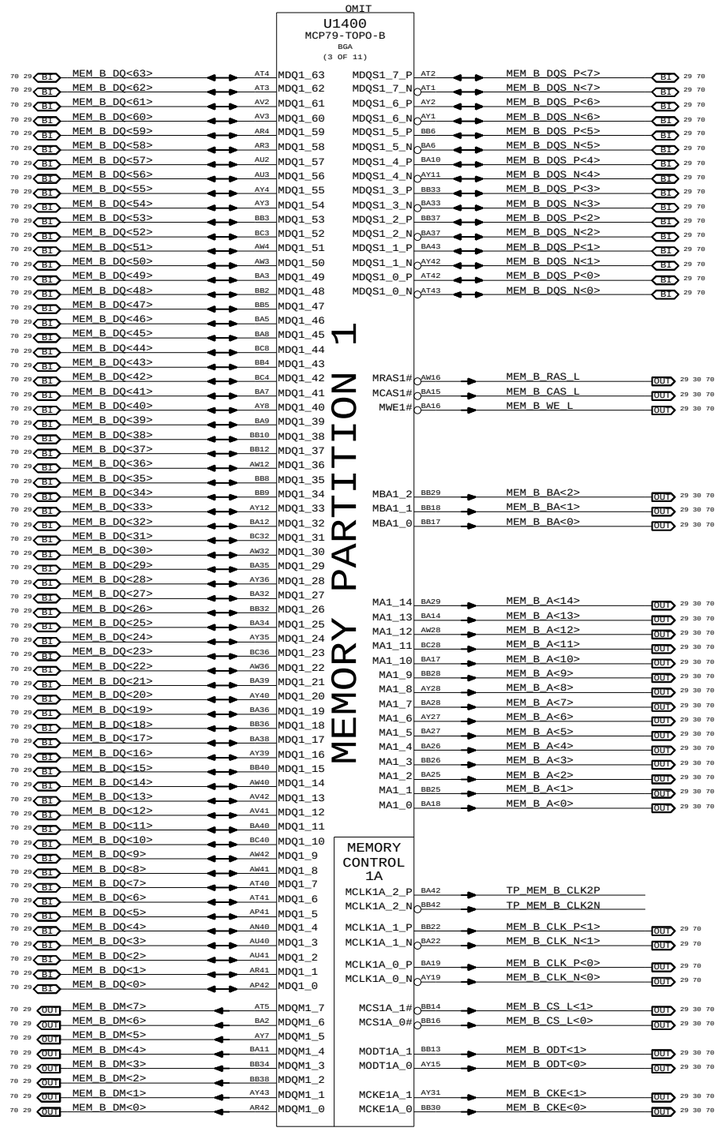

MCP Memory Interface

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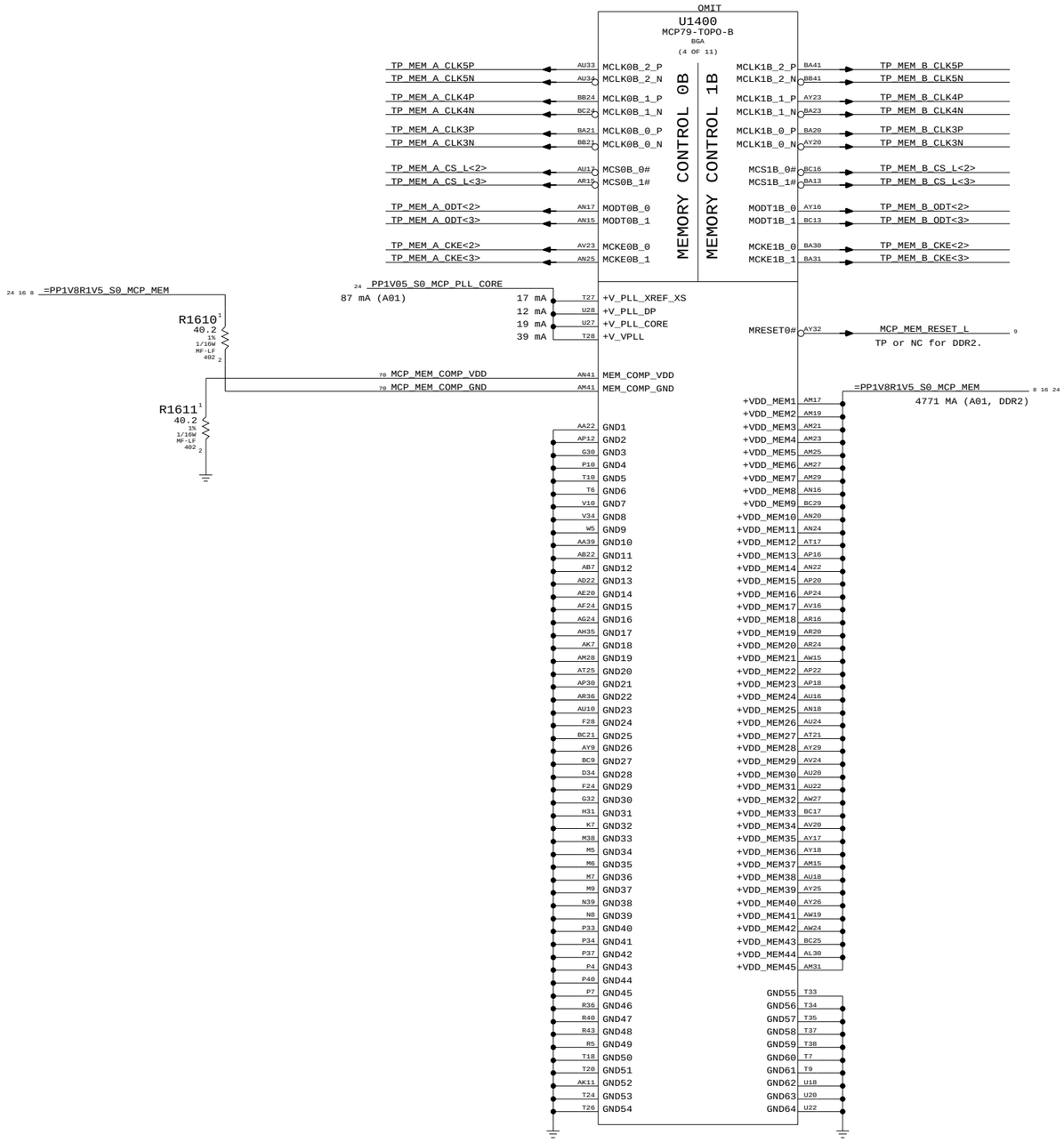

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MCP Memory Misc

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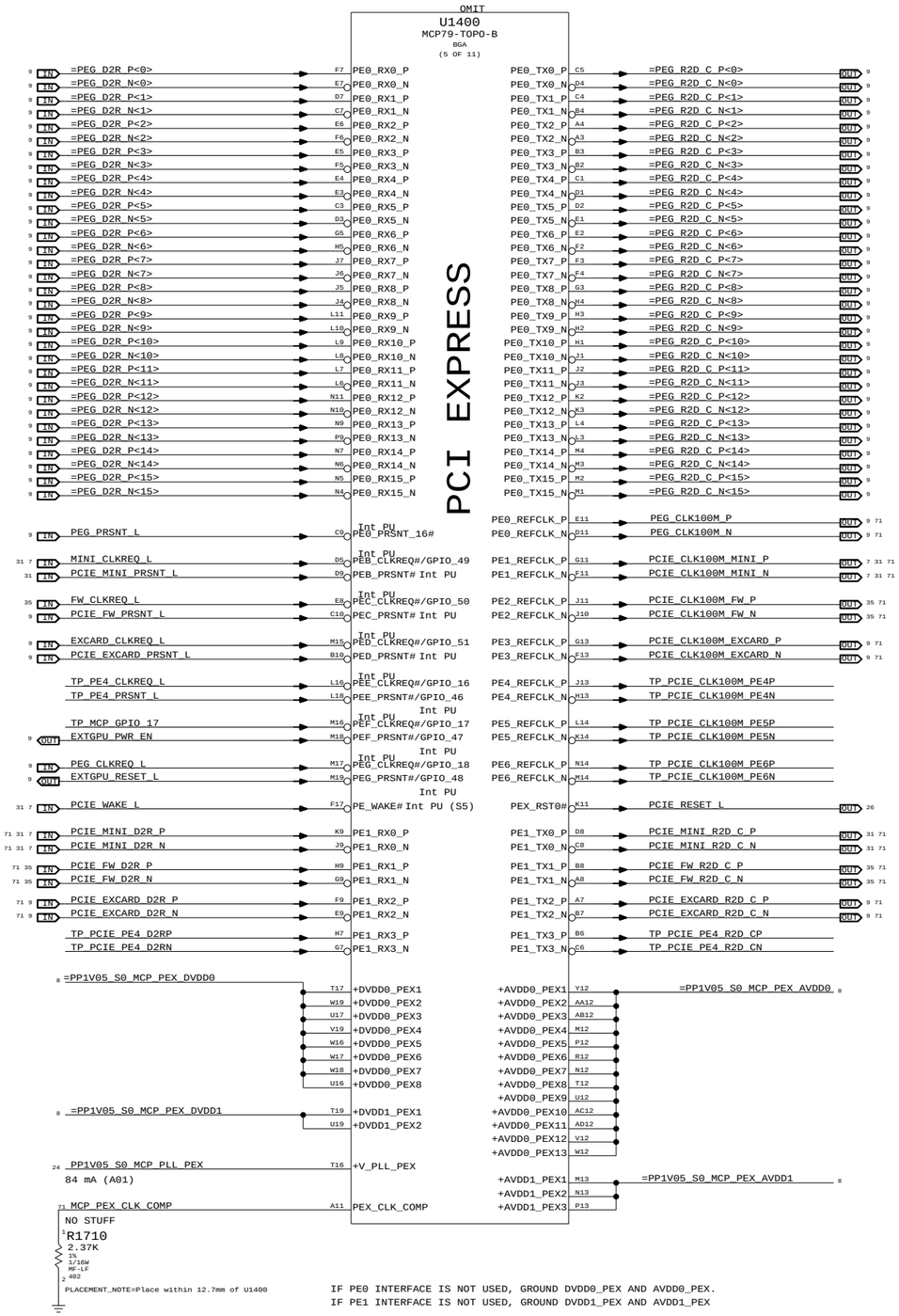

MCP PCIe Interfaces

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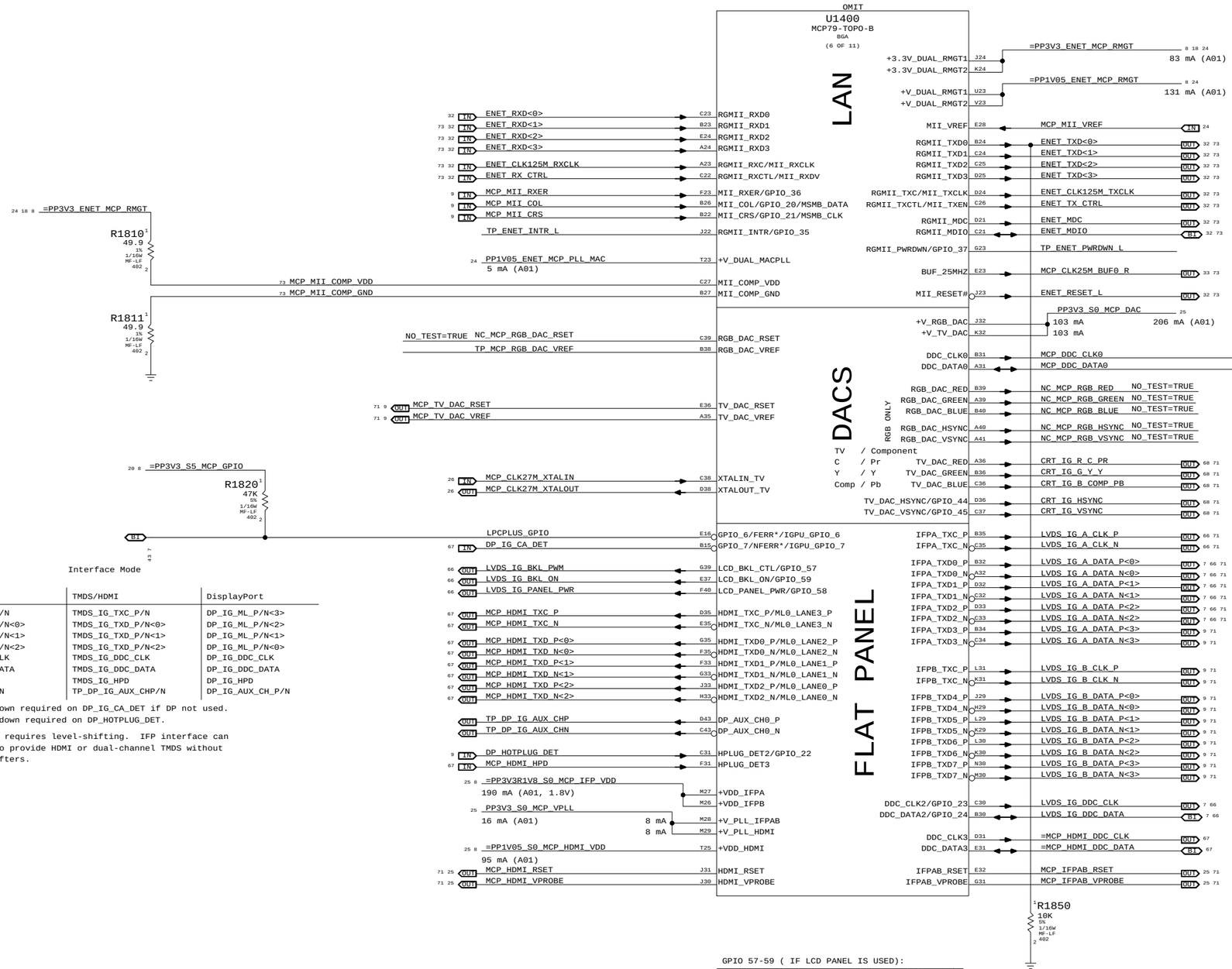

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OMIT

U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI

72 19	PCI_REQ0_L	T2	PCI_REQ0#		
72 19	PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2		
19 OUT	CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	PCI_GNT0# R3	TP_PCI_GNT0_L
9 OUT	AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	PCI_GNT1#/FANCTL2 U10	TP_PCI_GNT1_L
19 IN	MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	PCI_GNT2#/GPIO_41/RS232_DTR# R4	GMUX_JTAG_TMS OUT 9
				PCI_GNT3#/GPIO_39/RS232_RTS# U11	GMUX_JTAG_TDI OUT 9
				PCI_GNT4#/GPIO_53/RS232_SOUT# P3	MCP_RS232_SOUT_L OUT 19
72 13 7 BI	MCP_DEBUG<0>	AC3	PCI_AD0	PCI_CBE0# AA3	TP_PCI_C_BE_L<0>
72 13 7 BI	MCP_DEBUG<1>	AE10	PCI_AD1	PCI_CBE1# AA6	TP_PCI_C_BE_L<1>
72 13 7 BI	MCP_DEBUG<2>	AC4	PCI_AD2	PCI_CBE2# AA11	TP_PCI_C_BE_L<2>
72 13 7 BI	MCP_DEBUG<3>	AE11	PCI_AD3	PCI_CBE3# W10	TP_PCI_C_BE_L<3>
72 13 7 BI	MCP_DEBUG<4>	AB3	PCI_AD4		
72 13 7 BI	MCP_DEBUG<5>	AC6	PCI_AD5	PCI_DEVSEL# AA9	TP_PCI_DEVSEL_L
72 13 7 BI	MCP_DEBUG<6>	AB2	PCI_AD6	PCI_FRAME# Y4	TP_PCI_FRAME_L
72 13 7 BI	MCP_DEBUG<7>	AC7	PCI_AD7	PCI_IRDY# AA10	TP_PCI_IRDY_L
	TP_PCI_AD<8>	AC8	PCI_AD8	PCI_PAR Y1	TP_PCI_PAR
	TP_PCI_AD<9>	AA2	PCI_AD9	PCI_PERR#/GPIO_43/RS232_DCD# AB9	TP_PCI_PERR_L
	TP_PCI_AD<10>	AC9	PCI_AD10	PCI_SERR# AA7	TP_PCI_SERR_L
	TP_PCI_AD<11>	AC10	PCI_AD11	PCI_STOP# Y2	TP_PCI_STOP_L
	TP_PCI_AD<12>	AC11	PCI_AD12		
	TP_PCI_AD<13>	AA1	PCI_AD13	PCI_PME#/GPIO_30 T1	PM_LATRIGGER_L OUT 7 13
	TP_PCI_AD<14>	AA5	PCI_AD14	Int PU (S5)	
	TP_PCI_AD<15>	Y5	PCI_AD15		
	TP_PCI_AD<16>	W3	PCI_AD16	PCI_RESET0# R10	MEM_VTT_EN_R OUT 26
	TP_PCI_AD<17>	W6	PCI_AD17	PCI_RESET1# R11	TP_PCI_RESET1_L
	TP_PCI_AD<18>	W4	PCI_AD18		
	TP_PCI_AD<19>	W7	PCI_AD19		
	TP_PCI_AD<20>	V3	PCI_AD20	PCI_CLK0 R6	TP_PCI_CLK0
	TP_PCI_AD<21>	W8	PCI_AD21	PCI_CLK1 R7	TP_PCI_CLK1
	TP_PCI_AD<22>	V2	PCI_AD22	PCI_CLK2 R8	72 PCI_CLK33M_MCP_R
	TP_PCI_AD<23>	W9	PCI_AD23		
	TP_PCI_AD<24>	U3	PCI_AD24		
	TP_PCI_AD<25>	W11	PCI_AD25		
	TP_PCI_AD<26>	U2	PCI_AD26		
	TP_PCI_AD<27>	U5	PCI_AD27		
	TP_PCI_AD<28>	U1	PCI_AD28		
	TP_PCI_AD<29>	U6	PCI_AD29		
	TP_PCI_AD<30>	T5	PCI_AD30		
	TP_PCI_AD<31>	U7	PCI_AD31		
	TP_PCI_INTW_L	P2	PCI_INTW#		
	TP_PCI_INTX_L	N3	PCI_INTX#		
	TP_PCI_INTY_L	N2	PCI_INTY#		
	TP_PCI_INTZ_L	N1	PCI_INTZ#		
	TP_PCI_TRDY_L	Y3	PCI_TRDY#		
43 41 7 IN	PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42		
35 IN	FW_PME_L	AE2	LPC_DRQ1#/GPIO_19 Int PU		
	TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU		
43 41 7 BI	LPC_SERIRQ	AE6	LPC_SERIRQ Int PU		

R1910 22 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

PCI_CLKIN R9 — 72 PCI_CLK33M_MCP

LPC

LPC_FRAME#	AD4	LPC_FRAME_R_L	R1960 22 5% 1/16W MF-LF 402	LPC_FRAME_L	OUT 7 41 43 72
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12	LPC_PWRDWN_L			OUT 7 41 43
LPC_RESET0#	AE5	LPC_RESET_L			OUT 26 72
LPC_AD0	AD3	LPC_AD_R<0>	R1950 0 5% 1/16W MF-LF 402	LPC_AD<0>	BI 7 41 43 72
LPC_AD1	AD2	LPC_AD_R<1>	R1951 0 5% 1/16W MF-LF 402	LPC_AD<1>	BI 7 41 43 72
LPC_AD2	AD1	LPC_AD_R<2>	R1952 0 5% 1/16W MF-LF 402	LPC_AD<2>	BI 7 41 43 72
LPC_AD3	AD5	LPC_AD_R<3>	R1953 0 5% 1/16W MF-LF 402	LPC_AD<3>	BI 7 41 43 72
LPC_CLK0	AE9	LPC_CLK33M_SMC_R			OUT 26 72

R1961 10K 5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

GND65	U24	GND98	Y26
GND66	U26	GND99	Y27
GND67	U39	GND100	AB18
GND68	U4	GND101	H34
GND69	U8	GND102	AB20
GND70	V16	GND103	AB21
GND71	V17	GND104	AB23
GND72	V18	GND105	AB24
GND73	V20	GND106	AB25
GND74	V22	GND107	AB26
GND75	V24	GND108	AB27
GND76	V26	GND109	AB28
GND77	V27	GND110	AB34
GND78	V28	GND111	AB37
GND79	V33	GND112	AB4
GND80	V37	GND113	AB40
GND81	V4	GND114	AC22
GND82	V40	GND115	AC36
GND83	V7	GND116	AC40
GND84	W20	GND117	AB33
GND85	W22	GND118	AC5
GND86	W24	GND119	AD16
GND87	W36	GND120	AD17
GND88	W40	GND121	AD18
GND89	W43	GND122	AD19
GND90	Y16	GND123	AD20
GND91	Y17	GND124	AD24
GND92	Y18	GND125	AD25
GND93	Y19	GND126	AD26
GND94	Y20	GND127	AD27
GND95	Y22	GND128	AD28
GND96	Y24	GND129	AD33
GND97	Y25	GND130	AD34

21 18 8 =PP3V3_S0_MCP_GPIO

19 MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402
72 19 PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402
72 19 PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402
19 CRTMUX_SEL_TV_L	R1992	8.2K	5% 1/16W MF-LF 402
19 MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402

MCP PCI & LPC

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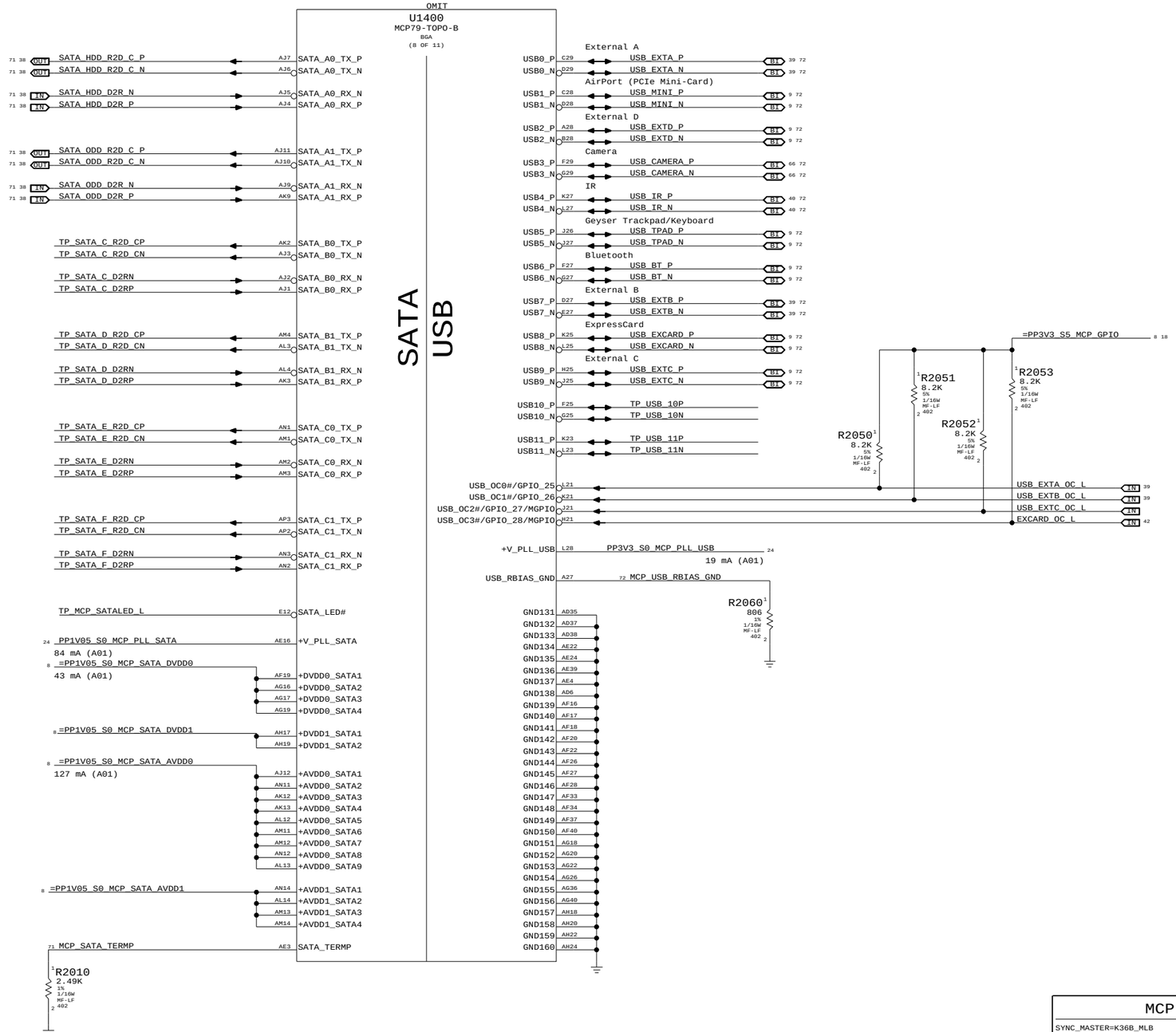

MCP SATA & USB

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SIZE	DRAWING NUMBER	REV.
D	051-8089	02

SCALE	SHT	OF
NONE	20	109

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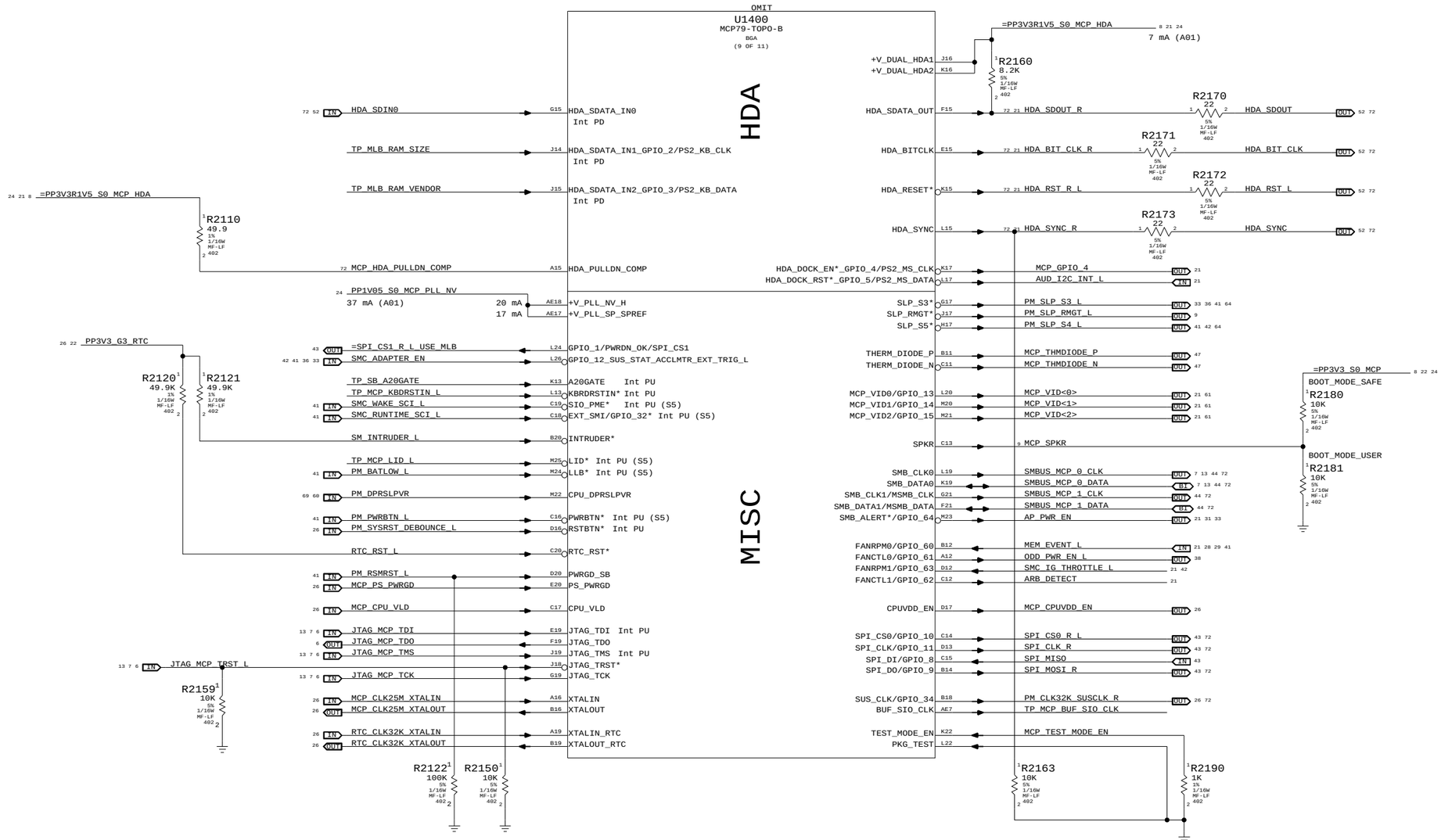


BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

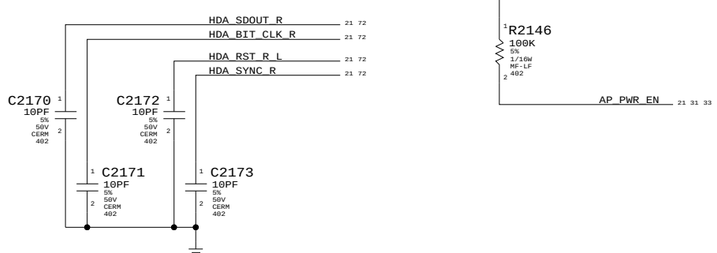
SPI Frequency Select

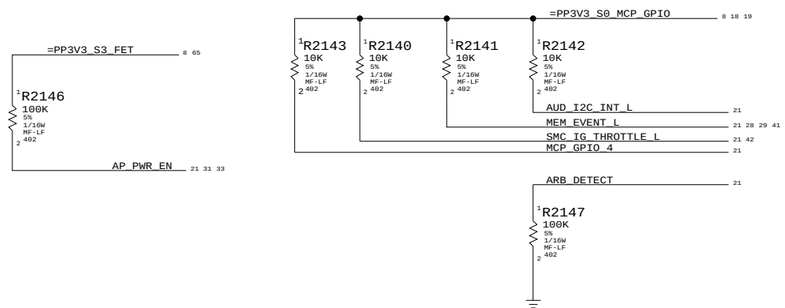
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

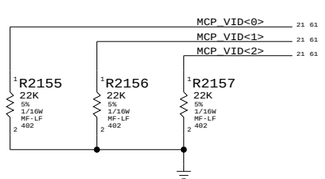
NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface







MCP HDA & MISC

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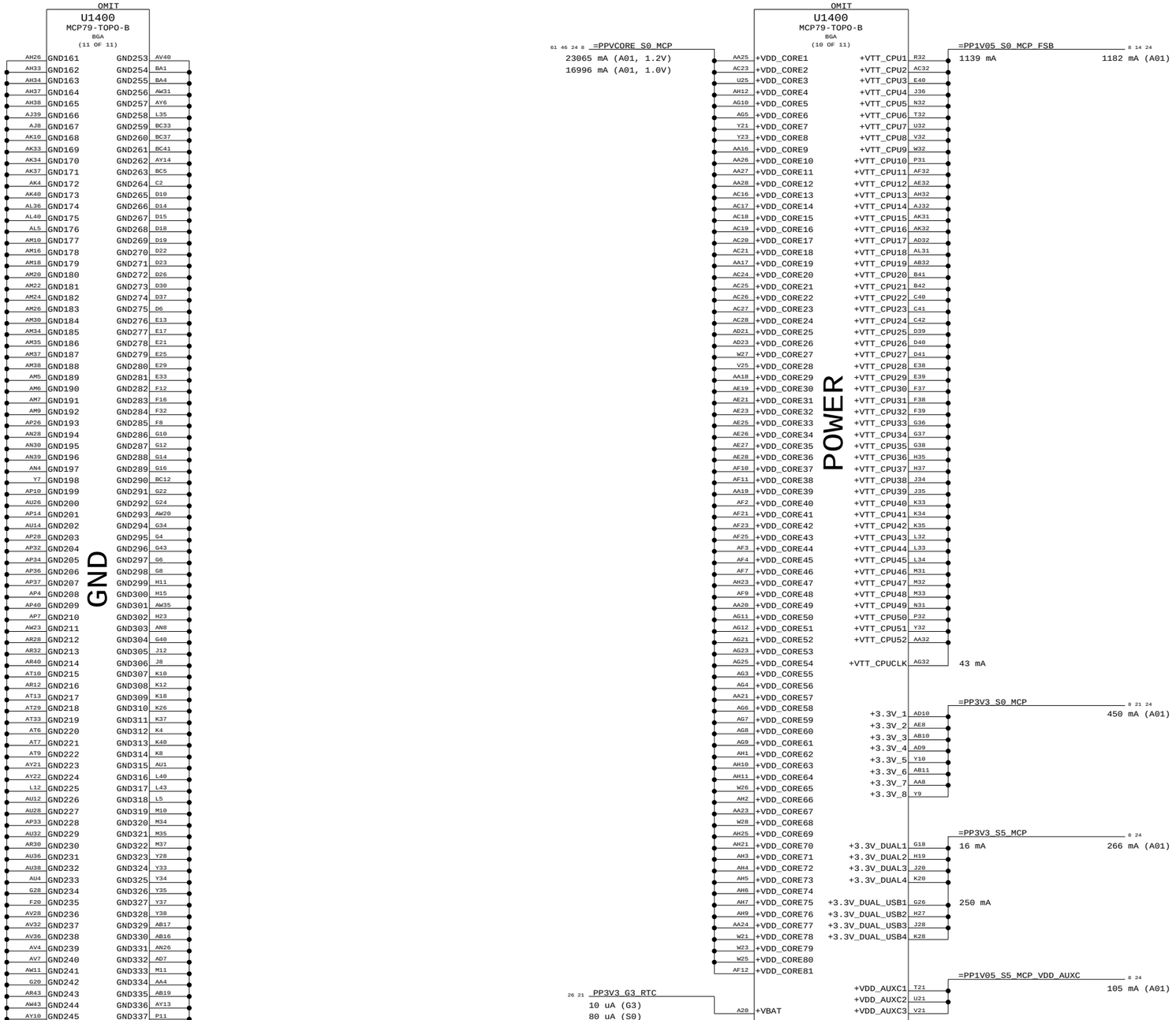

MCP Power & Ground

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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8	7	6	5	4	3	2	1

D

C

B

A

MCP79 A01 Silicon Support

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MCP Core Power

=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

=PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

=PP1V05_S0_MCP_FSB
1182 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

=PP1V8R1V5_S0_MCP_MEM
4771 MA (A01, DDR2)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

=PP3V3_S0_MCP
450 mA (A01)

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

=PP3V3_S0_MCP_PLL_UF
19 mA (A01)

L2555 30-OHM-1.7A 0402

PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

=PP3V3_S5_MCP
266 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

=PP3V3_ENET_MCP_RMGT
83 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2564 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2562 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef

=PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402

MCP_MII_VREF (OUT)

C2591 0.1UF 20% 10V CERM 402

=PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)

L2595 30-OHM-1.7A 0402

PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 0.1UF 20% 10V CERM 402

=PP1V05_S0_MCP_AVDD_UF
333 mA (A01)

L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

L2575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

=PP1V05_S0_MCP_PLL_UF
562 mA (A01)

L2580 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

C2580 4.7UF 20% 4V X5R 402
C2581 0.1UF 20% 10V CERM 402

L2582 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2582 4.7UF 20% 4V X5R 402
C2583 0.1UF 20% 10V CERM 402

L2584 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2584 4.7UF 20% 4V X5R 402
C2585 0.1UF 20% 10V CERM 402

L2586 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

C2586 4.7UF 20% 4V X5R 402
C2587 0.1UF 20% 10V CERM 402

L2588 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

C2588 4.7UF 20% 4V X5R 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

MCP Standard Decoupling

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SYNC_DATE=08/17/2008

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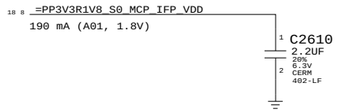
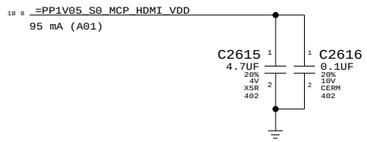
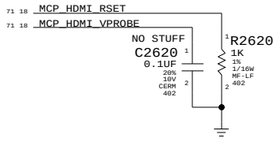
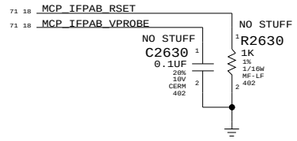
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

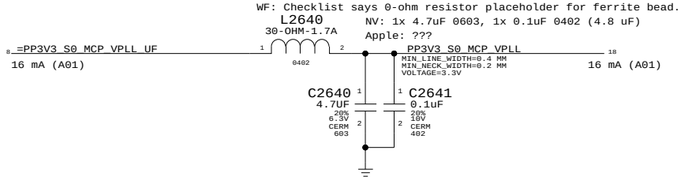




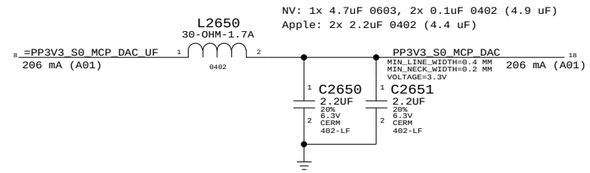




WF: Checklist says 0-ohm resistor placeholder for ferrite bead.



NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)



HDCP ROM

WF: Open question on which packge option(s) nVidia can support.

SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672

MCP Graphics Support

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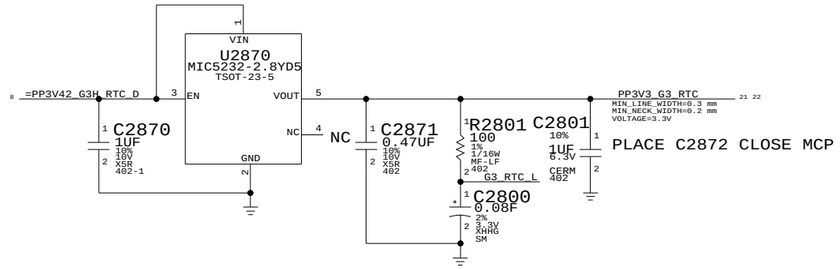
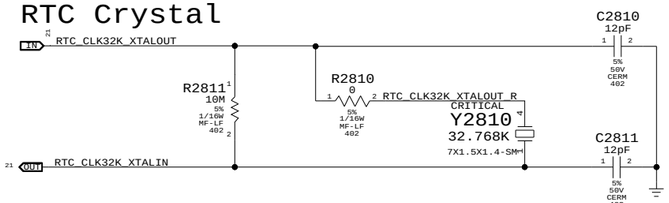
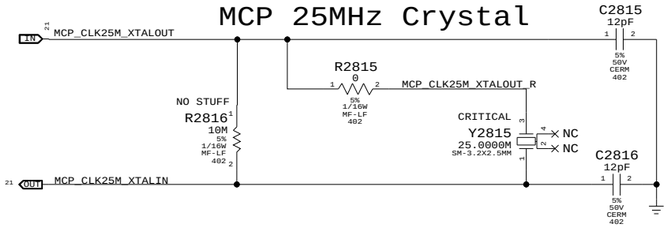
RTC Power Sources



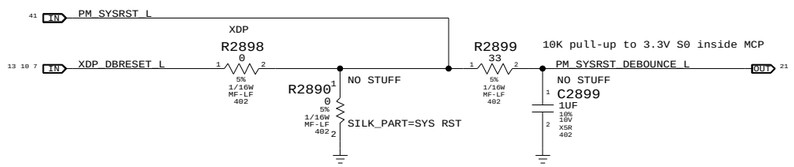
RTC Crystal



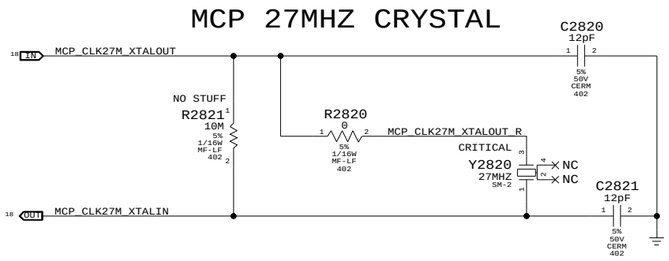
MCP 25MHz Crystal



Reset Button

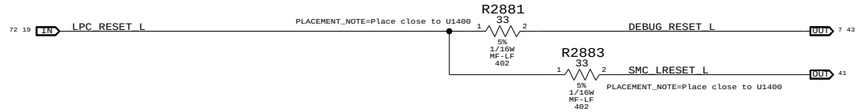


MCP 27MHZ CRYSTAL

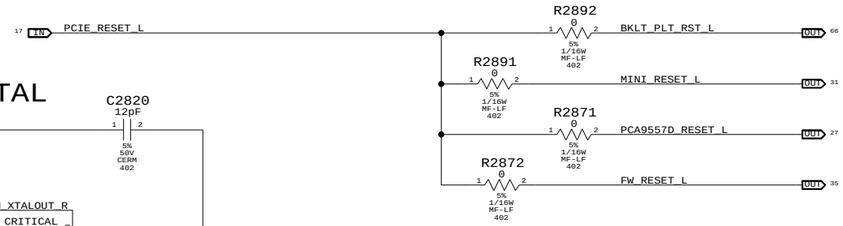


Platform Reset Connections

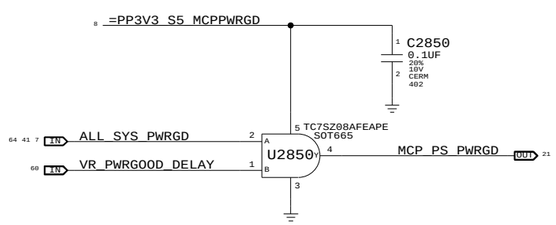
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



MCP S0 PWRGD



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC POWER SOURCE FROM COIN CELL TO SUPER CAPS
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SB Misc

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Page Notes

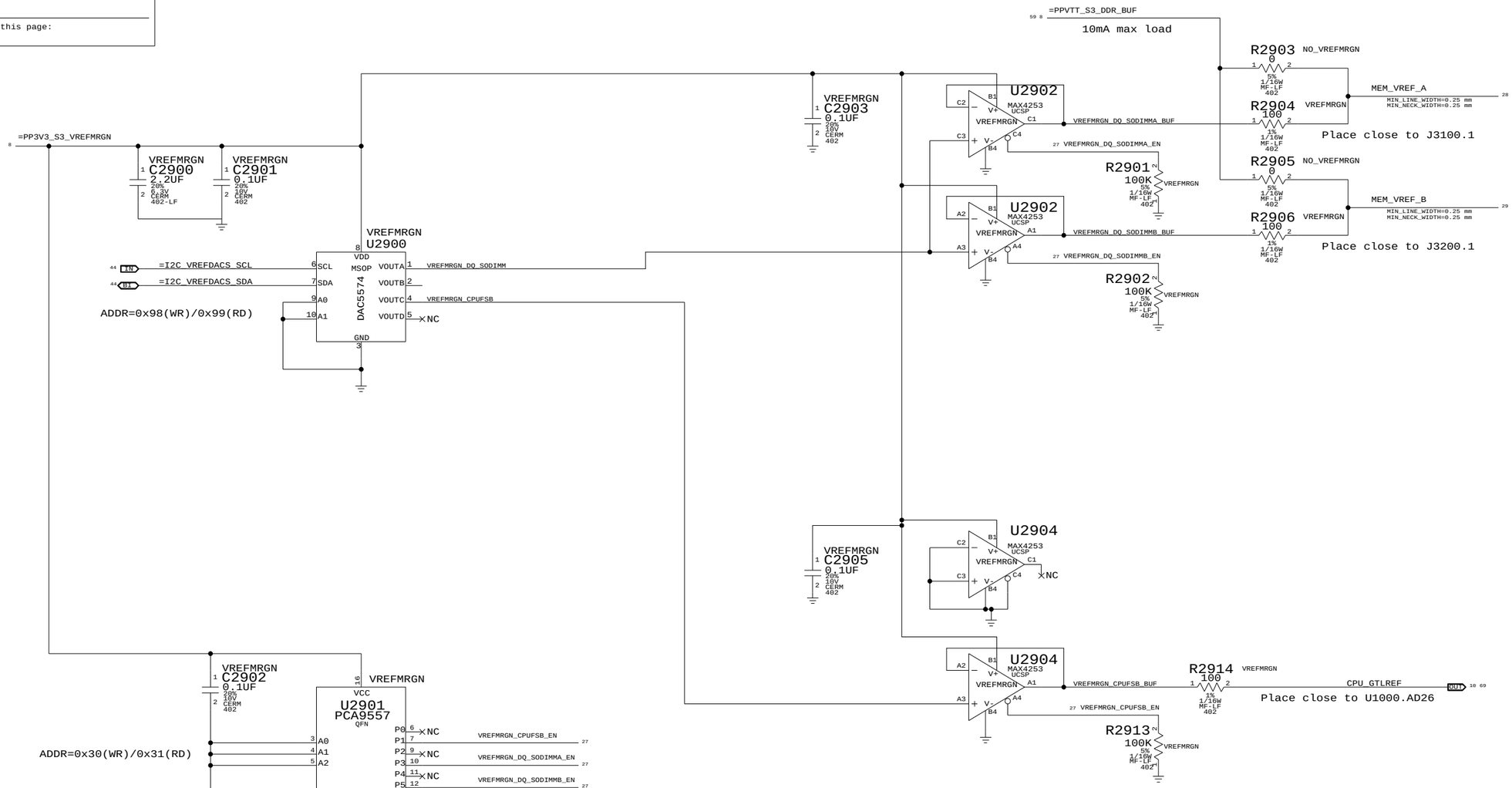
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN AND NO VERFMRGN

Voltage divider resistor values at op-amp outputs not yet finalized.

BOM OPTION TO SELECT VREF SOURCE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0149	1	RES, MTL FILM, 200, 1%, 0402, SM, LF	R2903		VREFMRGN
114S0149	1	RES, MTL FILM, 200, 1%, 0402, SM, LF	R2905		VREFMRGN

FSB/DDR2 VREF MARGINING

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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D	051-8089	02
SCALE: NONE	SHT 29 OF 109	

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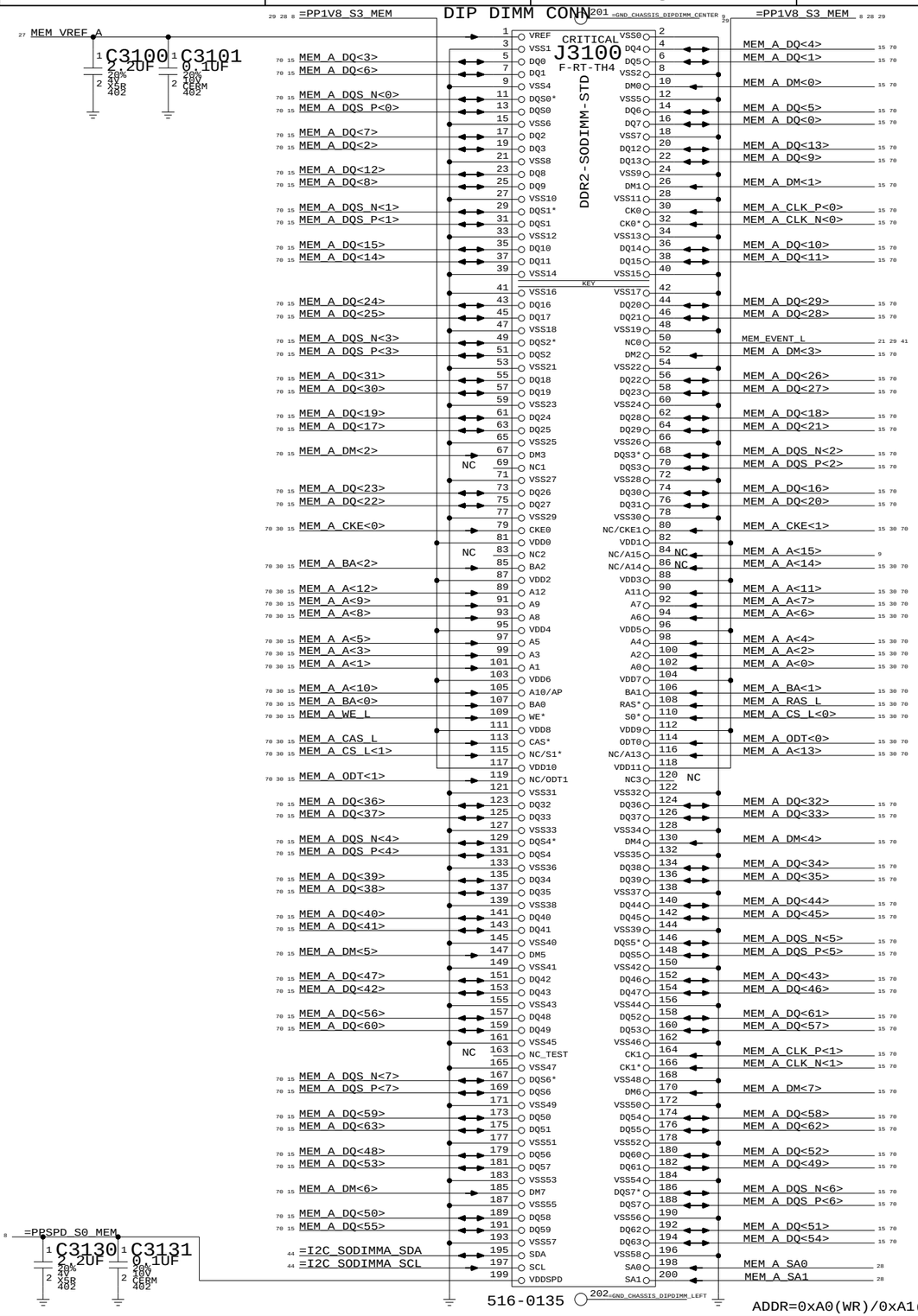


Page Notes

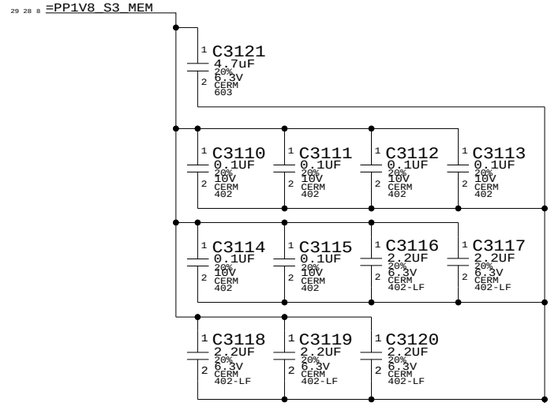
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

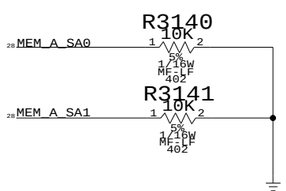
BOM options provided by this page:
(NONE)

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



DDR2-800

DDR2 SO-DIMM Connector A			
SYNC_MASTER=K36B_MLB		SYNC_DATE=08/17/2008	
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	SCALE NONE	SHT 31 OF 109	

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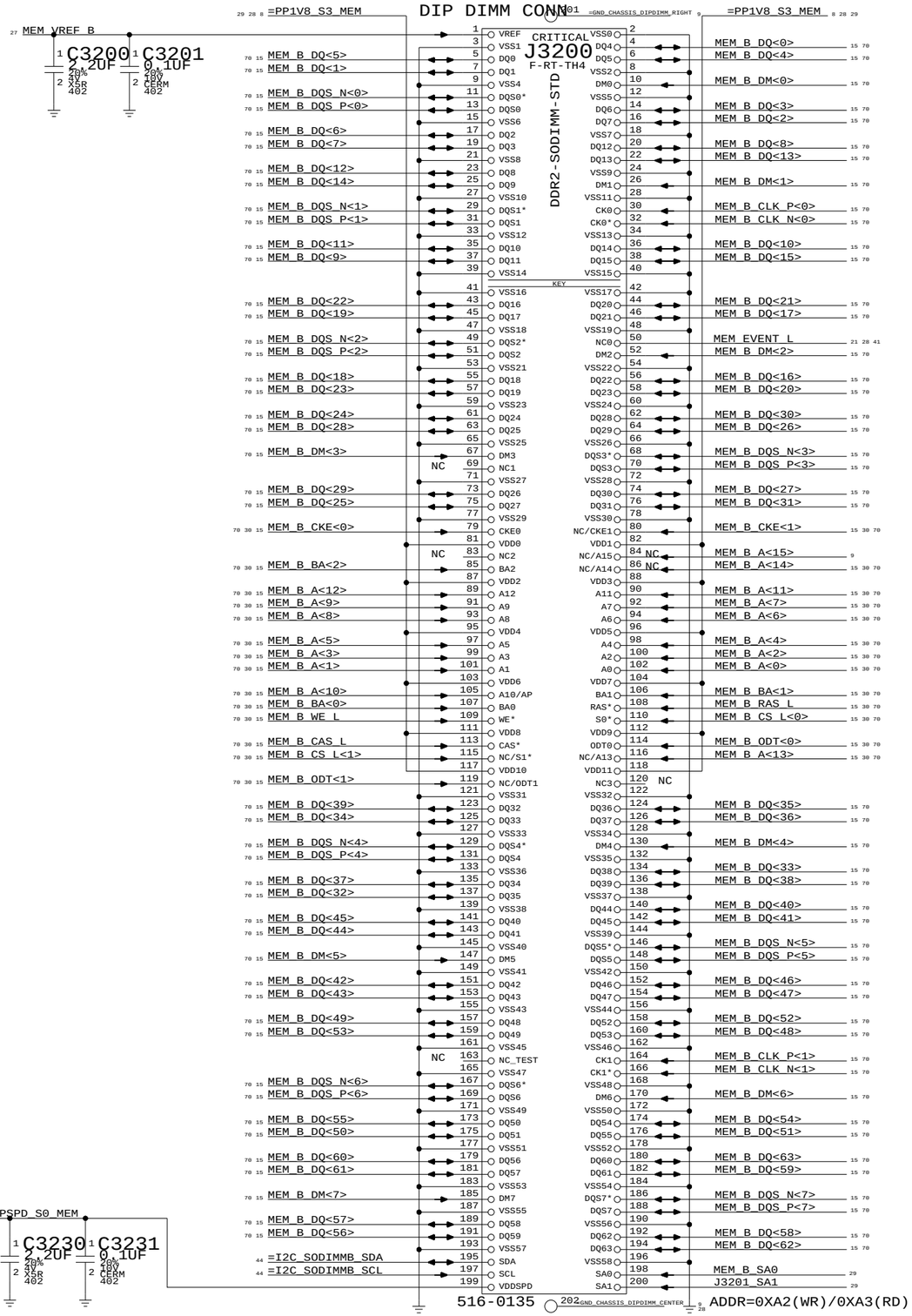

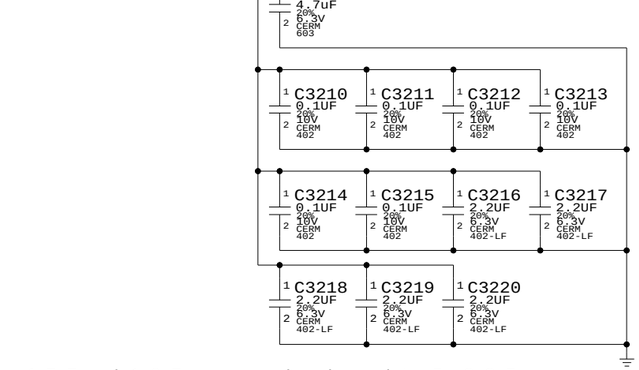

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

DDR2 Bypass Caps

(For return current)

The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

=PPSPD_S0_MEM
R3241 10K 5% 1/16W MF-LF 402
MEM_B_SA0
J3201_SA1
R3240 10K 5% 1/16W MF-LF 402

Resistor prevents pwr-gnd short

DDR2-800

DDR2 SO-DIMM Connector B

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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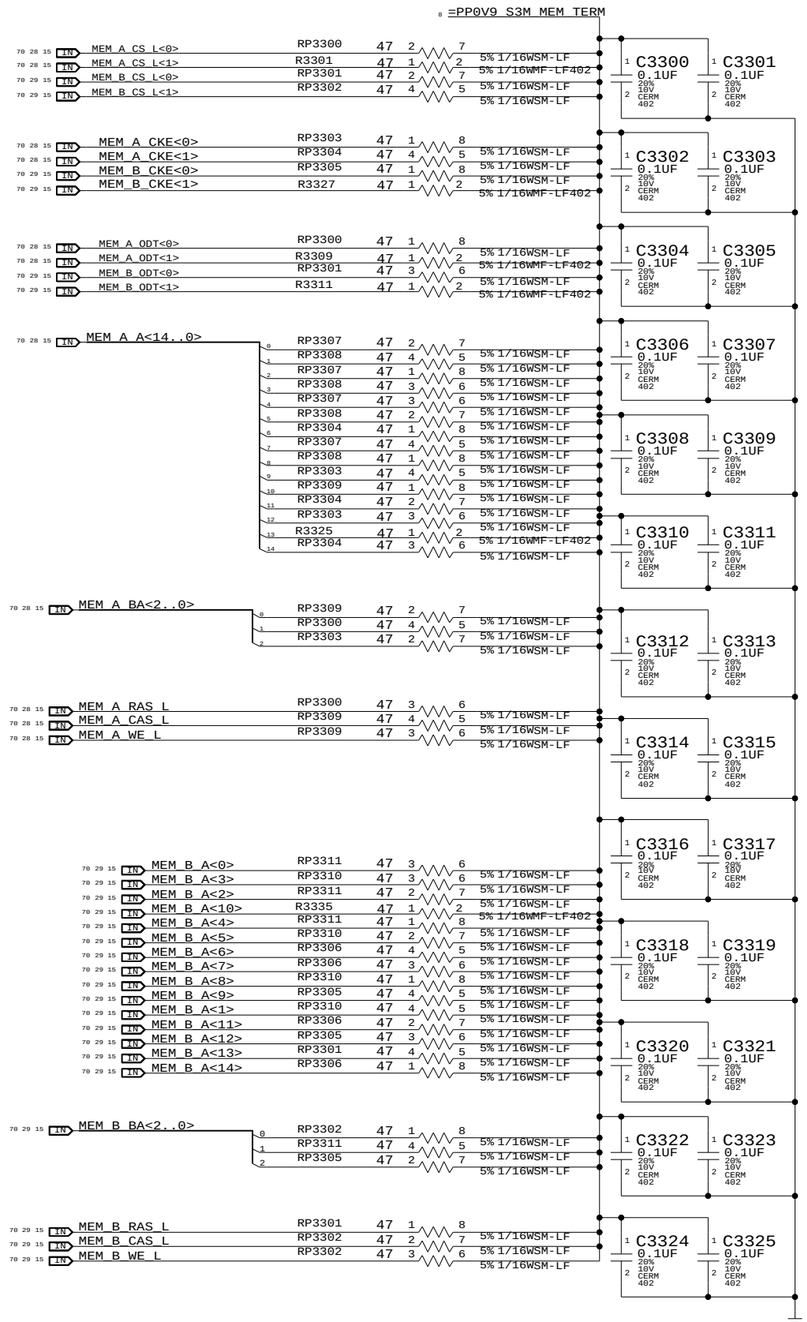
One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

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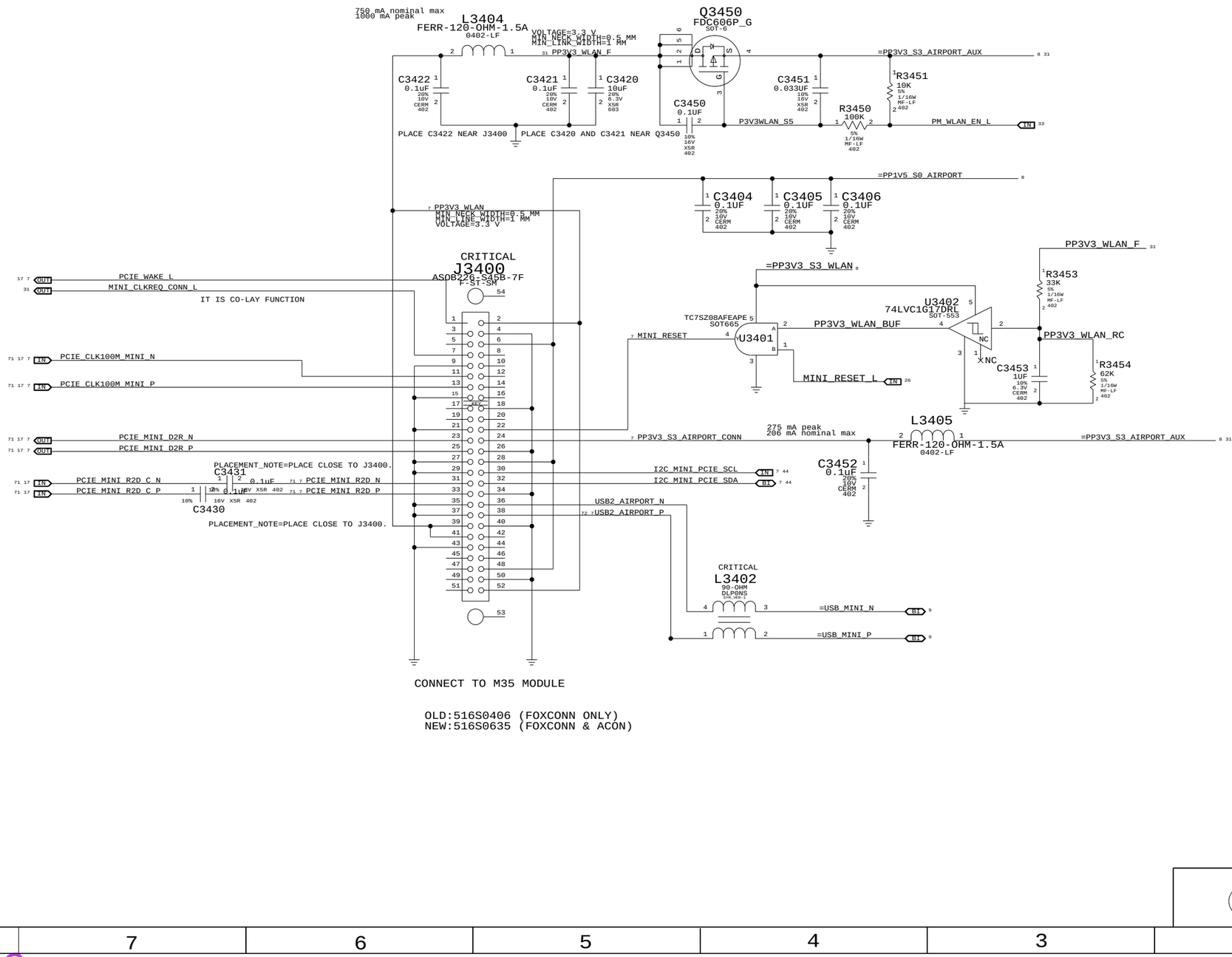
AIRPORT



CONNECT TO M35 MODULE

OLD:516S0406 (FOXCONN ONLY)
NEW:516S0635 (FOXCONN & ACON)

Right Clutch Connector

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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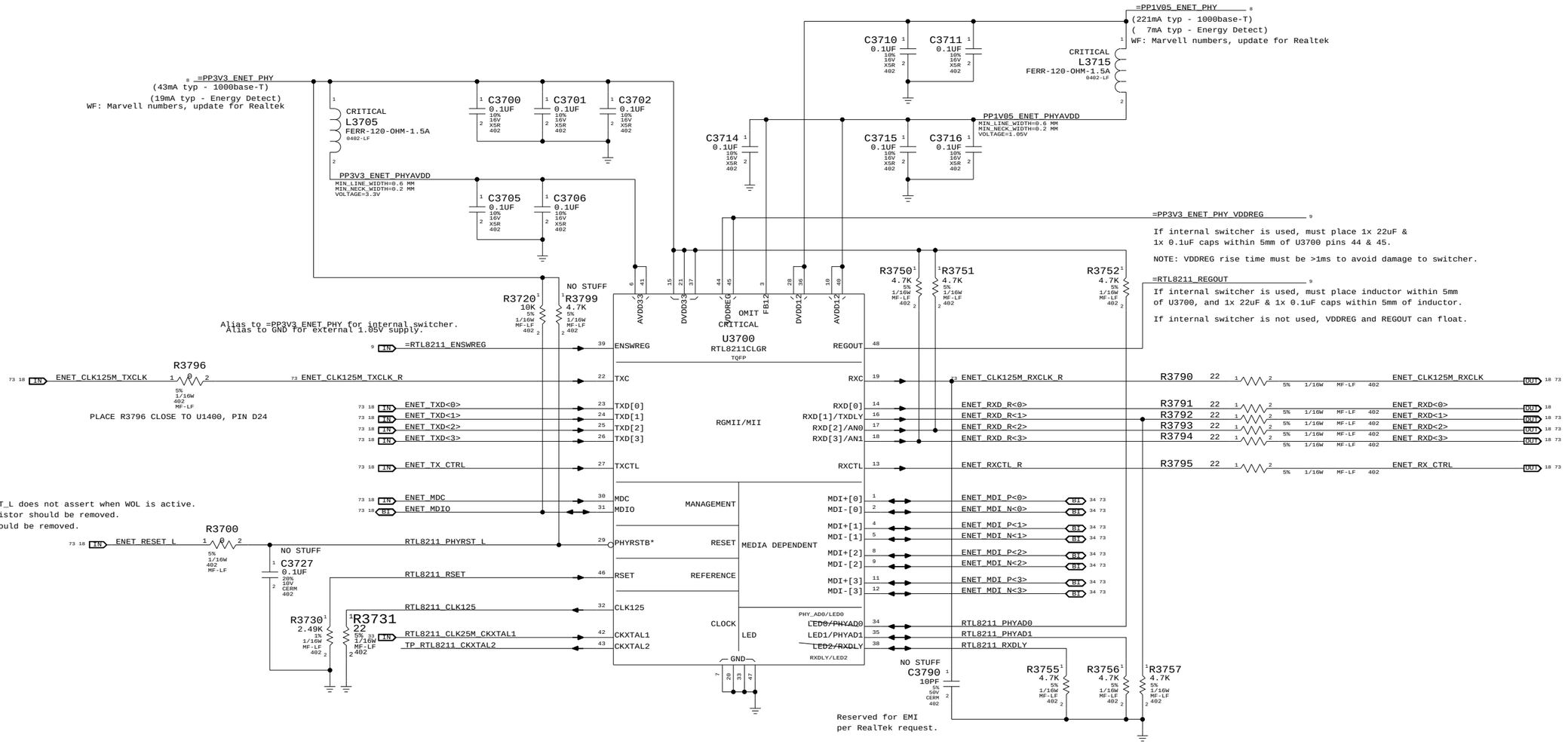

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA SYNC_DATE=03/20/2008

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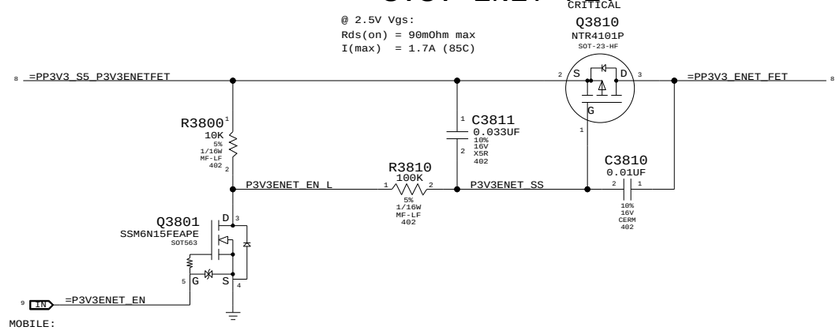
3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)



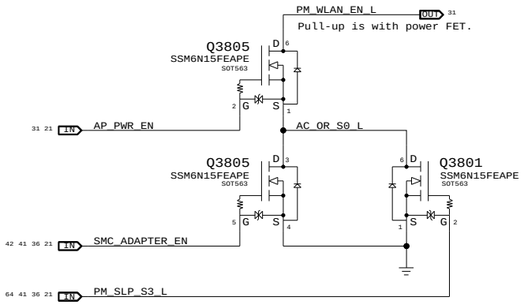
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

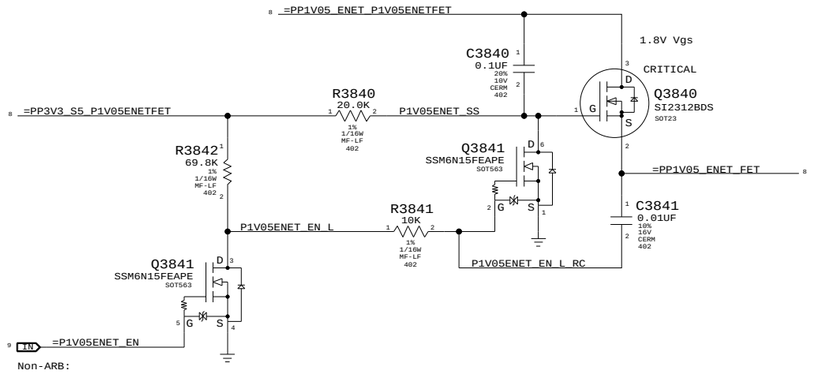
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET

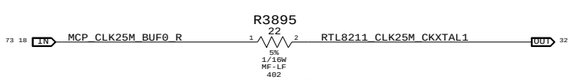


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=SUMA SYNC_DATE=04/04/2008

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- COPY THIS PAGE FROM K36 CSA.39

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902

ENET_CONN_CTAP

C3900 0.1UF 10% 16V X5R 402
C3901 0.1UF 10% 16V X5R 402
C3902 0.1UF 10% 16V X5R 402
C3903 0.1UF 10% 16V X5R 402

CRITICAL
T3901
SM
TLA-6T213HF
TX
RX

CRITICAL
T3902
SM
TLA-6T213HF
TX
RX

R3903 75 1% 1/16W MF-LF 402
R3902 75 1% 1/16W MF-LF 402
R3901 75 1% 1/16W MF-LF 402
R3900 75 1% 1/16W MF-LF 402

ENET_MDI_P<1>	T3901 pin 1	T3901 pin 12	ENET_MDI_TRAN_P<1>
ENET_MDI_N<1>	T3901 pin 2	T3901 pin 11	ENET_MDI_TRAN_N<1>
ENET_CENTER_TAP<1>	T3901 pin 3	R3903	
ENET_CENTER_TAP<3>	T3901 pin 4	R3902	
ENET_MDI_P<3>	T3901 pin 5	T3901 pin 8	ENET_MDI_TRAN_P<3>
ENET_MDI_N<3>	T3901 pin 6	T3901 pin 7	ENET_MDI_TRAN_N<3>
ENET_MDI_N<2>	T3902 pin 1	T3902 pin 12	ENET_MDI_TRAN_N<2>
ENET_MDI_P<2>	T3902 pin 2	T3902 pin 11	ENET_MDI_TRAN_P<2>
ENET_CENTER_TAP<2>	T3902 pin 3	R3901	
ENET_CENTER_TAP<0>	T3902 pin 4	R3900	
ENET_MDI_N<0>	T3902 pin 5	T3902 pin 8	ENET_MDI_TRAN_N<0>
ENET_MDI_P<0>	T3902 pin 6	T3902 pin 7	ENET_MDI_TRAN_P<0>

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C3910 1000PF 10% 2KV CERM 1206

9 =GND_CHASSIS_RJ45

ETHERNET CONNECTOR

OMIT
CRITICAL
J3900
RJ45-MG3-K36
F-RT-TH

1	ENET_MDI_TRAN_P_0
2	ENET_MDI_TRAN_N_0
3	ENET_MDI_TRAN_P_1
4	ENET_MDI_TRAN_N_1
5	ENET_MDI_TRAN_P_2
6	ENET_MDI_TRAN_N_2
7	ENET_MDI_TRAN_P_3
8	ENET_MDI_TRAN_N_3
9, 10	CHASSIS

514-0523

ETHERNET CONNECTOR

SYNC_MASTER=SUMA SYNC_DATE=04/04/2008

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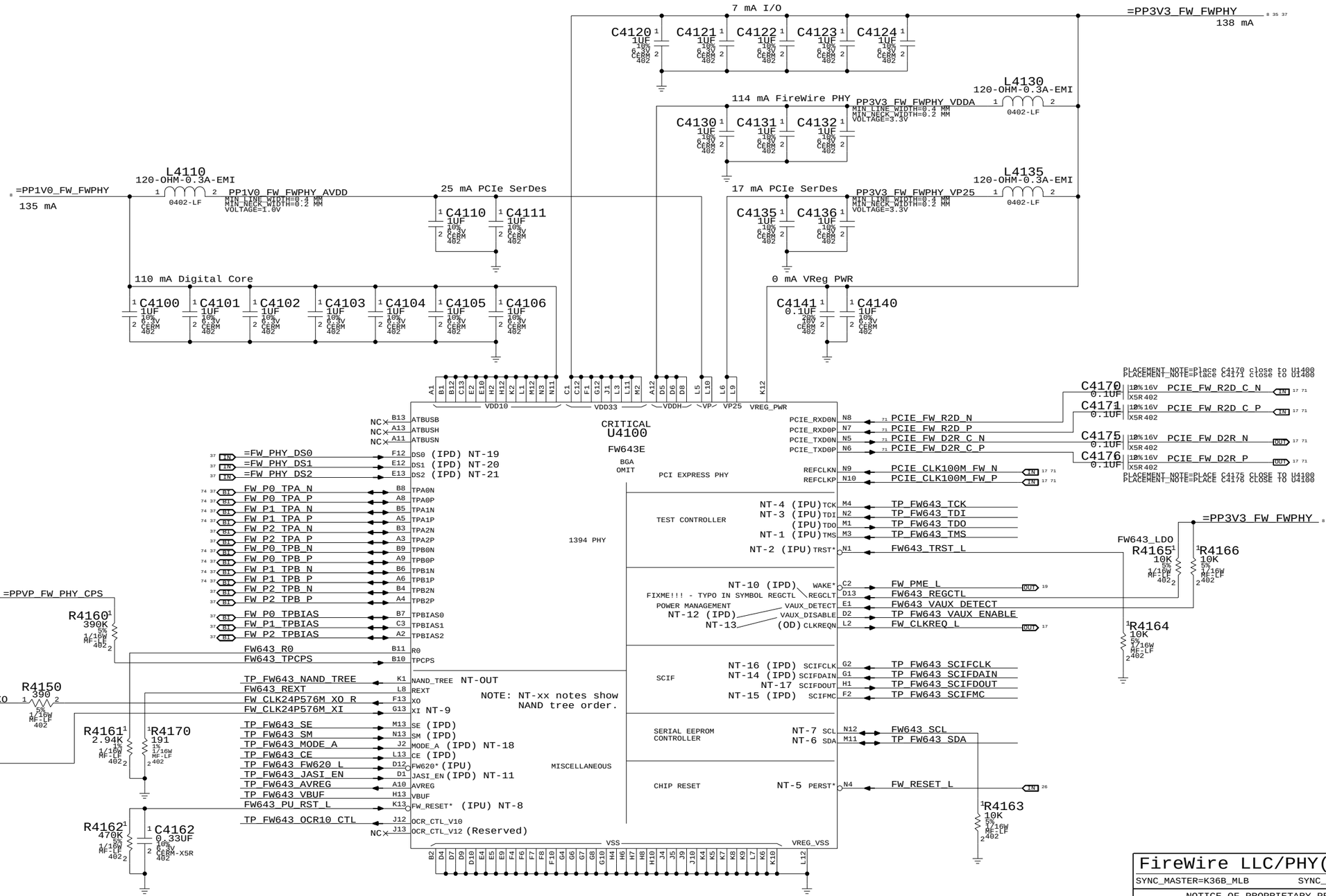

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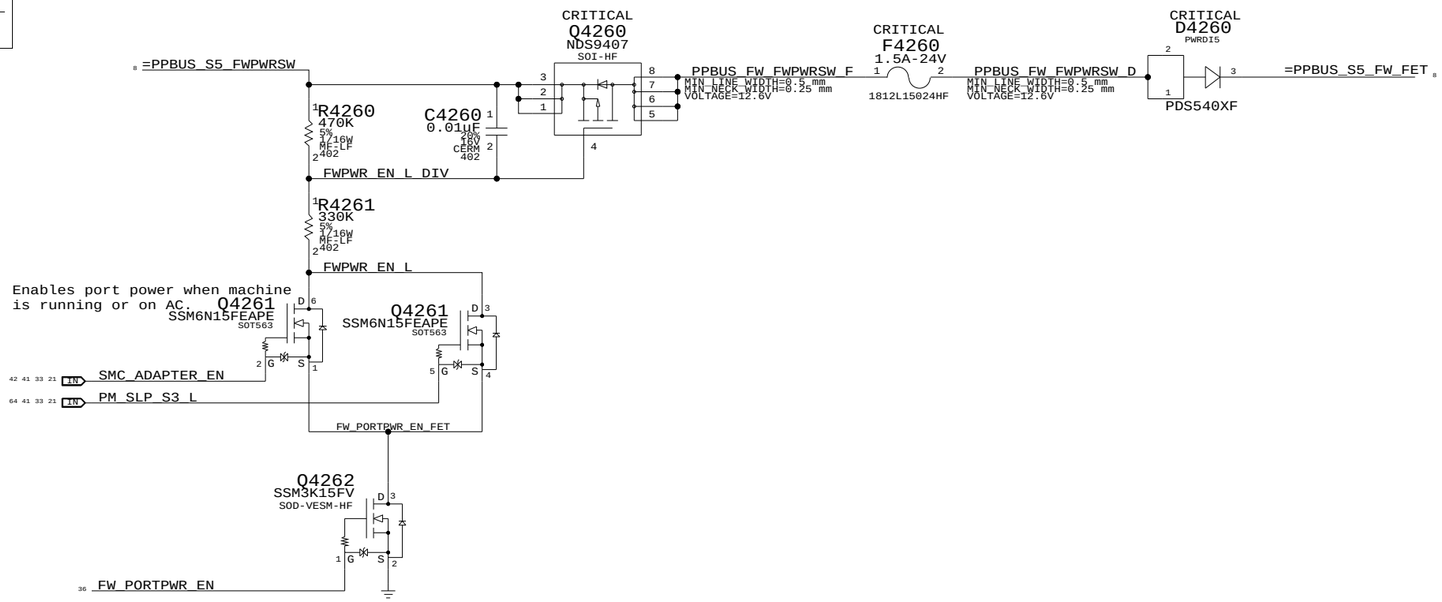
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

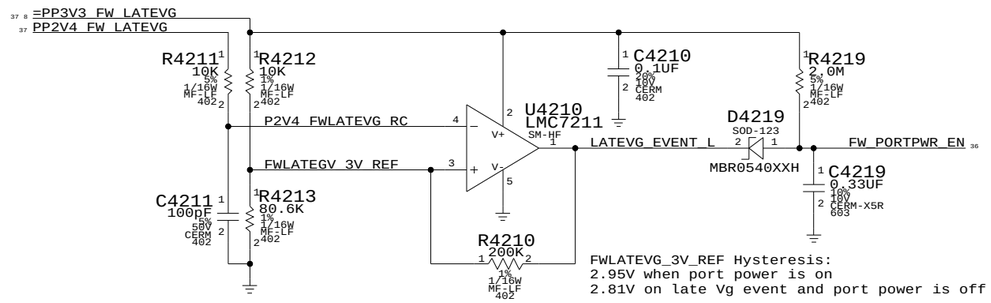
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:
- 1-port Portable Power Class (0)

=PP3V3_FW_PHY

R4381 10K 5% 1/10W MF-LF 402
R4382 10K 5% 1/10W MF-LF 402
R4380 10K 5% 1/10W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE = =FW_PHY_DS0
FWPHY_DS2 MAKE_BASE=TRUE = =FW_PHY_DS2
FWPHY_DS1 MAKE_BASE=TRUE = =FW_PHY_DS1

OUT

FW_P0_TPBIAS = NC_FW0_TPBIAS MAKE_BASE=TRUE
FW_P2_TPBIAS = NC_FW2_TPBIAS MAKE_BASE=TRUE
FW_P0_TPA_N = NC_FW0_TPAN MAKE_BASE=TRUE
FW_P0_TPA_P = NC_FW0_TPAP MAKE_BASE=TRUE
FW_P2_TPA_N = NC_FW2_TPAN MAKE_BASE=TRUE
FW_P2_TPA_P = NC_FW2_TPAP MAKE_BASE=TRUE

FW_P0_TPB_N = NC_FW0_TPBN MAKE_BASE=TRUE
FW_P0_TPB_P = NC_FW0_TPBP MAKE_BASE=TRUE
FW_P2_TPB_N = NC_FW2_TPBN MAKE_BASE=TRUE
FW_P2_TPB_P = NC_FW2_TPBP MAKE_BASE=TRUE

Termination

Place close to FireWire PHY

FW_P1_TPBIAS
C4360 0.33UF 10% 6.3V CERM-X5R 402

R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/10W MF-LF 402

FW_P1_TPA_P = FW_PORT1_TPA_P MAKE_BASE=TRUE
FW_P1_TPA_N = FW_PORT1_TPA_N MAKE_BASE=TRUE
FW_P1_TPB_P = FW_PORT1_TPB_P MAKE_BASE=TRUE
FW_P1_TPB_N = FW_PORT1_TPB_N MAKE_BASE=TRUE

R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/10W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/10W MF-LF 402

=PPVP_FW_PHY_CPS_FET
Q4300 BSS8402DW SOT-363
PPVP_FW_CPS MAKE_BASE=TRUE = =PPVP_FW_PHY_CPS

R4311 470K 5% 1/10W MF-LF 402

CPS_EN_L_DIV

R4312 330K 5% 1/10W MF-LF 402

CPS_EN_L

=PP3V3_FW_FWPHY
Q4300 BSS8402DW SOT-363 (SYM-VER1)

Cable Power

CRITICAL
L4310 FERR-250-OHM NOTE: TRACE PPVP_FW_PORT1 MUST HANDLE UP TO 1A
=PPVP_FW_PORT1
SM
PPVP_FW_PORT1_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

"Snapback" & "Late VG" Protection

PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363
C4311 0.01uF 10% 50V X7R 402
C4310 0.01uF 10% 50V X7R 402

FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N

CRITICAL
FL4320 TCM2010-100-4P SM

FW_PORT_A_P
FW_PORT_A_N
FW_PORT_B_P
FW_PORT_B_N

CRITICAL
PORT 1
J4300 1394A-MG3-K36 F-RT-TH

TPA+
TPA-
TPB+
TPB-
POWER
GROUND
=GND_CHASSIS_FW_UPPER
=GND_CHASSIS_FW_DOWN

C4316 0.01UF 10% 50V X7R 402

DP4311 BAV99DW-X-G SOT-363
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402

Late-VG Protection Power

=PP3V3_FW_LATEVG
R4390 332 1% 1/16W MF-LF 402
PP2V4_FW_LATEVG
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.4V

CRITICAL
D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

FireWire Ports

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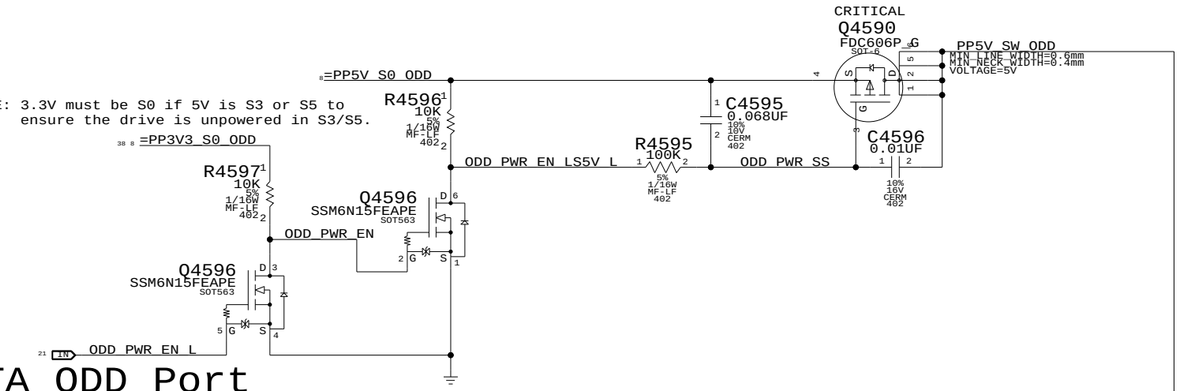
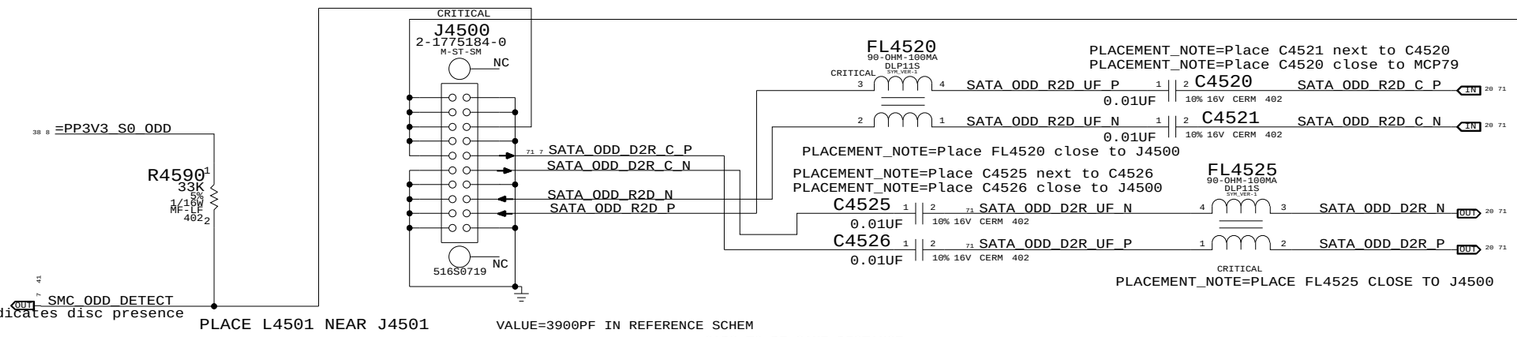
ODD Power Control

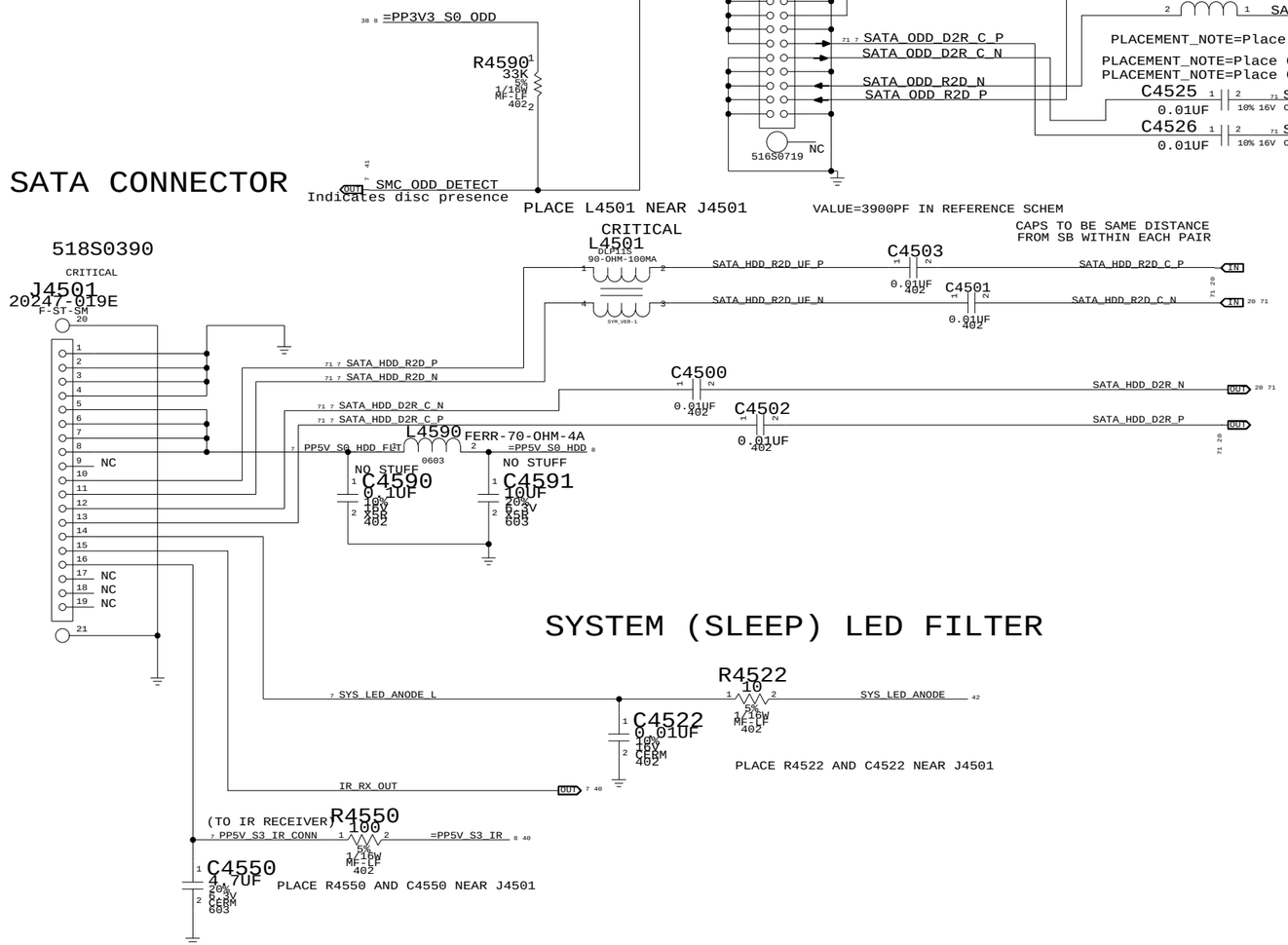
NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.



SATA ODD Port



SATA CONNECTOR



SYSTEM (SLEEP) LED FILTER

SATA Connectors

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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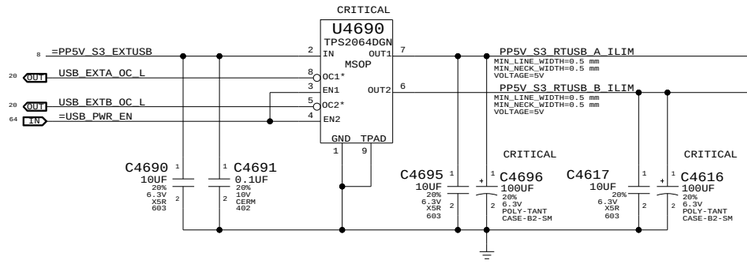
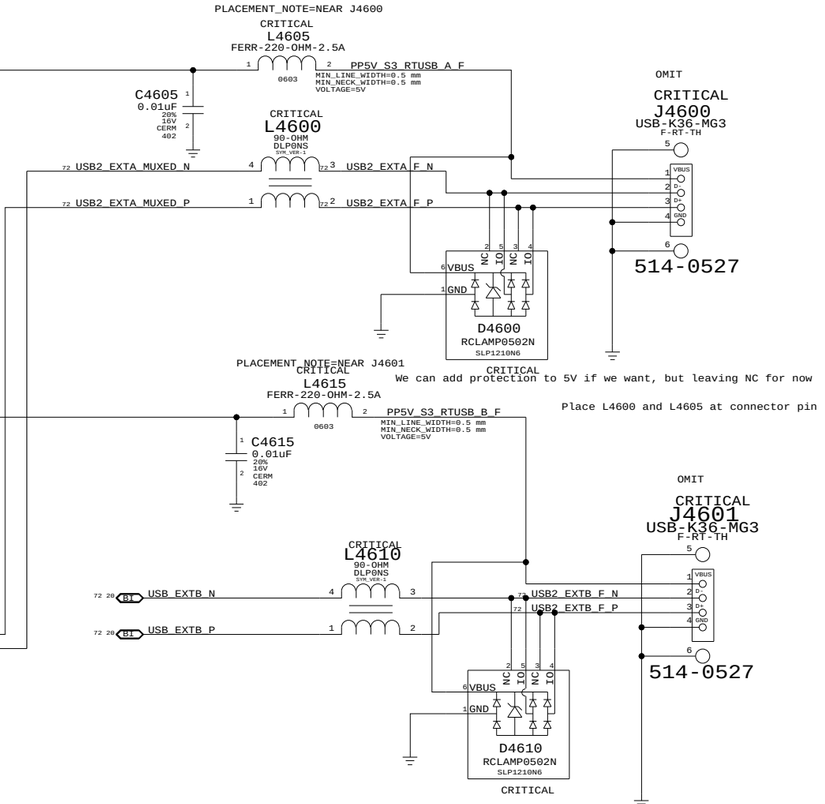
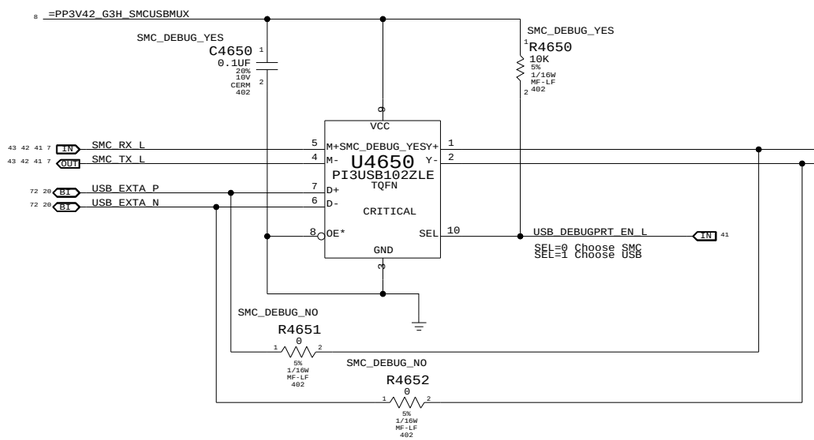
Port Power Switch



Left USB Port A



USB/SMC Debug Mux



Left USB Port B

External USB Connectors

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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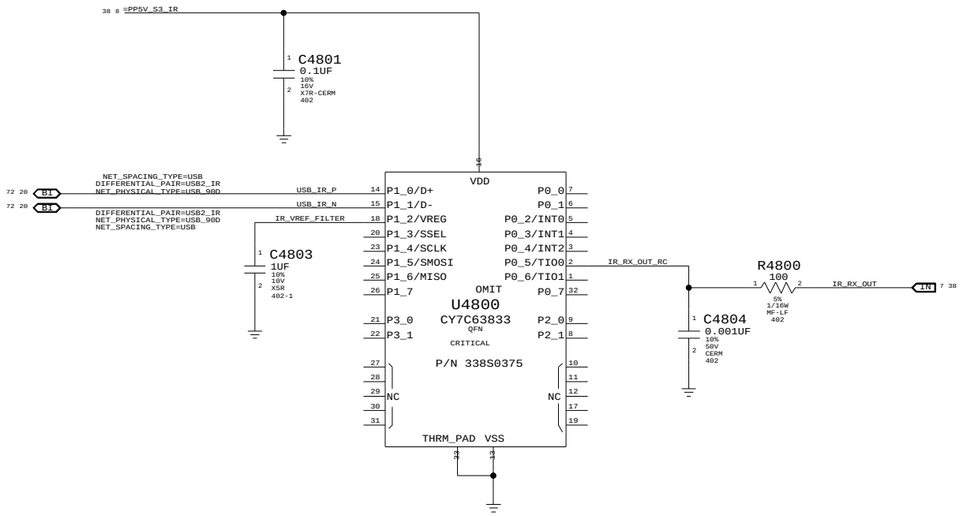
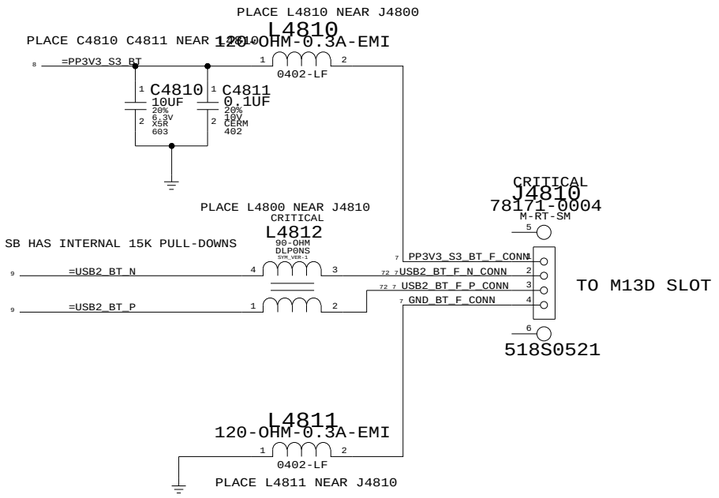
IR CTRL



CYPRESS 'ENCORE II' USB CONTROLLER

BLUETOOTH



Front Flex Support

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NONE	48	109

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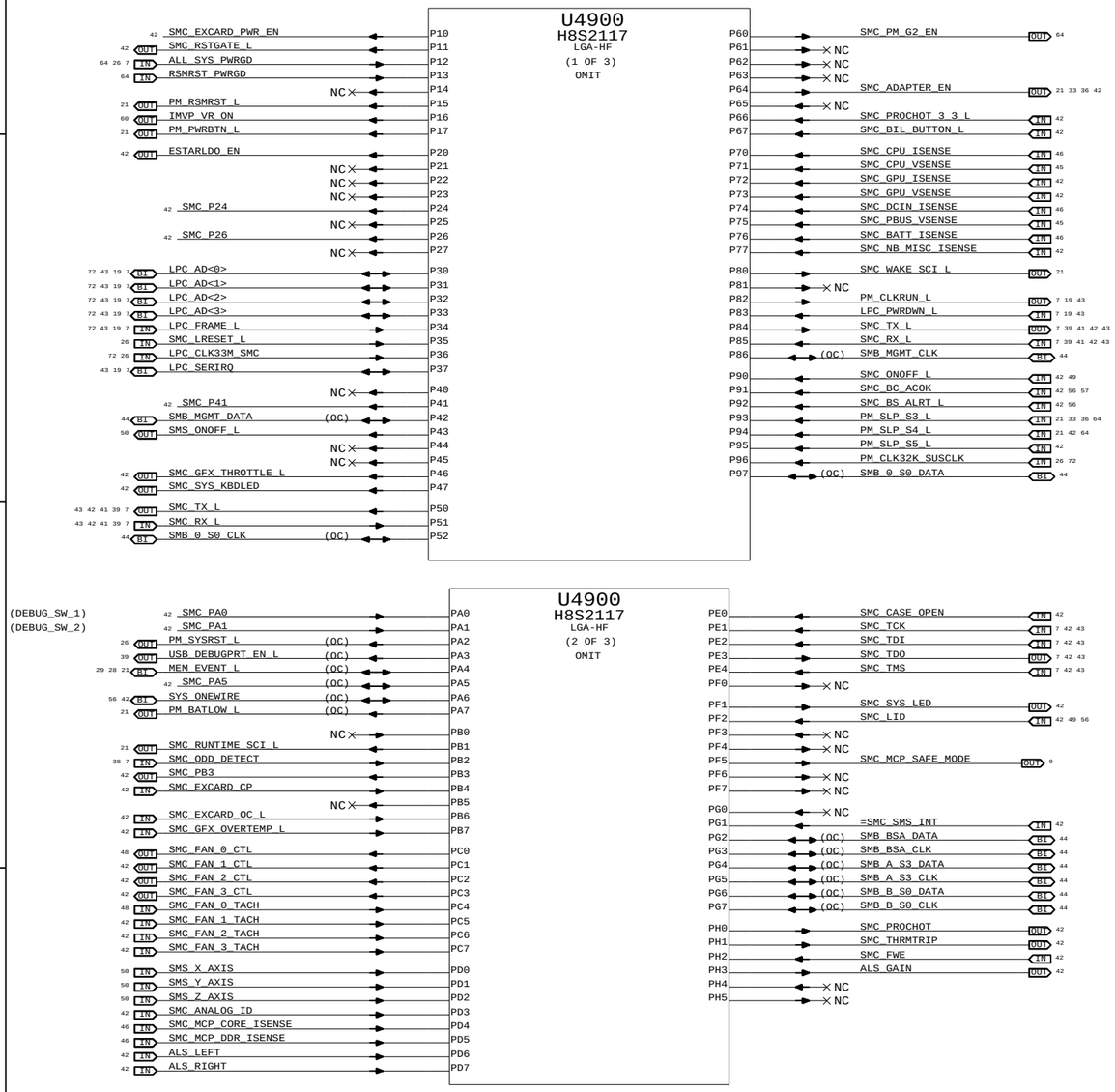
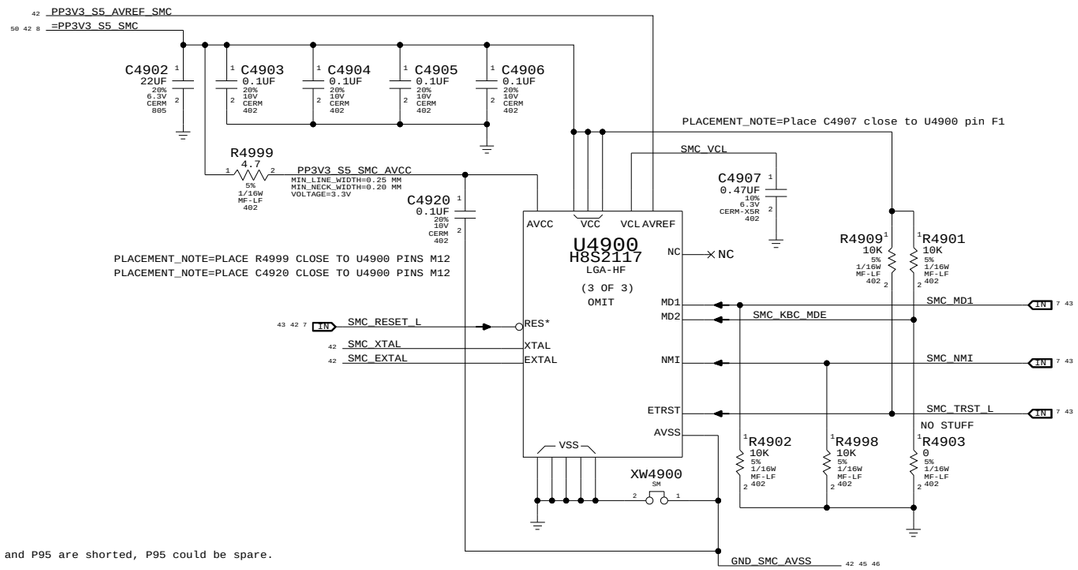
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC

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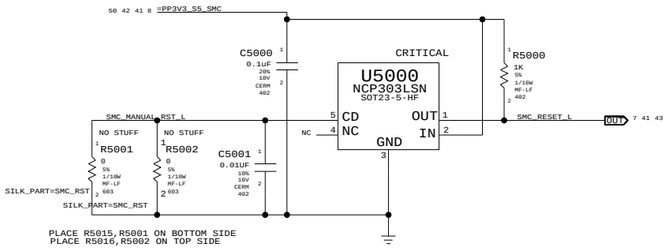
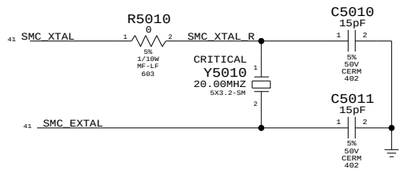
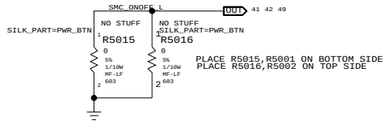
SMC Reset "Button" / Brownout Detect



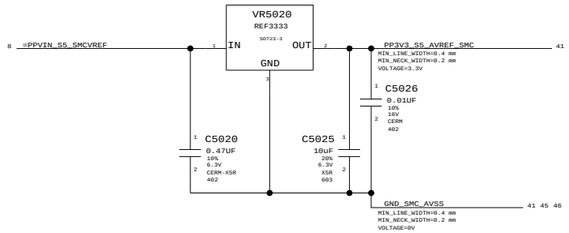
SMC Crystal Circuit



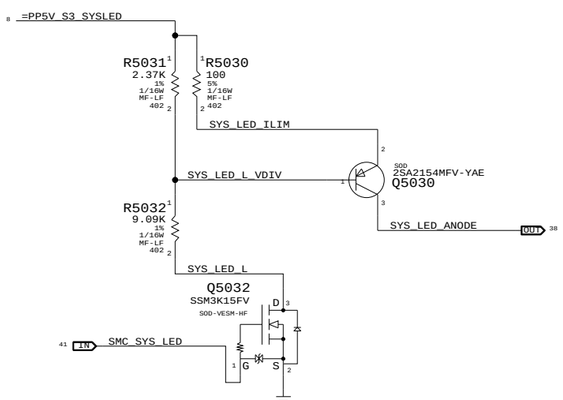
Debug Power "Button"



SMC AVREF Supply



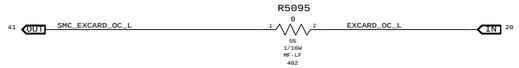
System (Sleep) LED Circuit



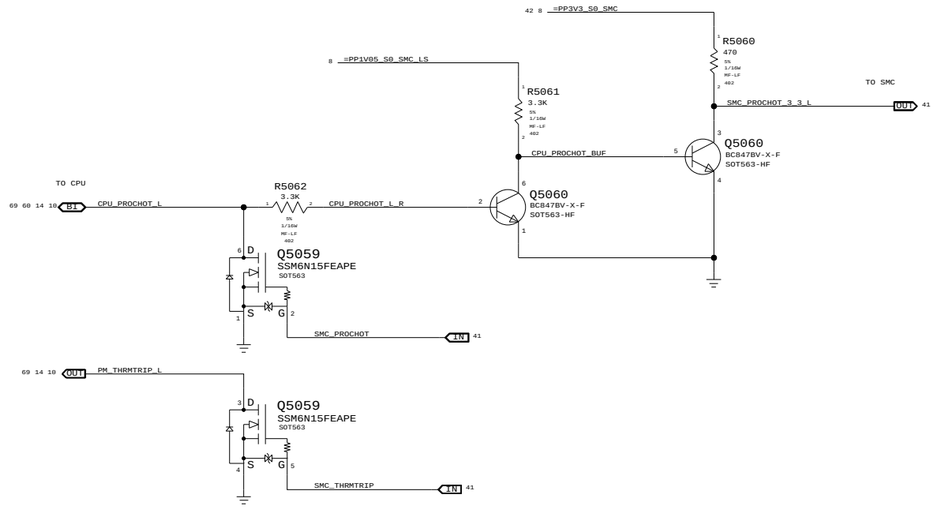
ADD NC ALIASES FOR FAN1 SIGNALS

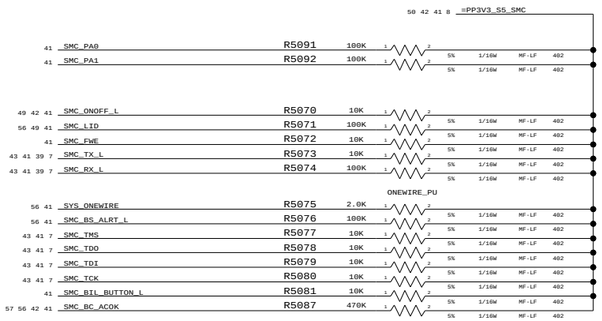
41 SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE NO_TEST=TRUE
41 SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE NO_TEST=TRUE
41 SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE NO_TEST=TRUE
41 SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE NO_TEST=TRUE
41 SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE NO_TEST=TRUE
41 SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE NO_TEST=TRUE
41 SMC_GFX_OVERTEMP_L	TP_SMC_GFX_OVERTEMP_L	MAKE_BASE=TRUE
41 SMC_GFX_THROTTLE_L	SMC_IG_THROTTLE_L 21	MAKE_BASE=TRUE
57 56 42 41 SMC_BC_ACOK	=CHGR_ACOK	MAKE_BASE=TRUE
41 ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE

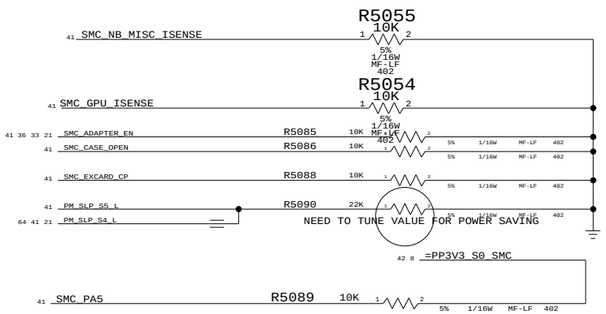
41 SMC_PB3	NC_SMC_PB3	MAKE_BASE=TRUE
41 SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE
41 SMC_P26	SMC_BMON_MUX_SEL 46	MAKE_BASE=TRUE
41 SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE
41 SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE
41 SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE
41 ALS_RIGHT	NC_ALS_RIGHT	MAKE_BASE=TRUE NO_TEST=TRUE
41 ESTARLDO_EN	NC_ESTARLDO_EN	MAKE_BASE=TRUE NO_TEST=TRUE
41 SMC_ANALOG_ID	NC_SMC_ANALOG_ID	MAKE_BASE=TRUE NO_TEST=TRUE
41 SMC_SYS_KBDLED	NC_SMC_SYS_KBDLED	MAKE_BASE=TRUE NO_TEST=TRUE
41 =SMC_SMS_INT	SMS_INT_L 50	MAKE_BASE=TRUE
45 SMC_MCP_VSENSE	SMC_GPU_VSENSE 41	
46 SMC_CPU_FSB_ISENSE	ALS_LEFT 41	



SMC FSB to 3.3V Level Shifting






R5055 10K 5% 1/16W MF-LF 402
41 SMC_NB_MISC_ISENSE
R5054 10K 5% 1/16W MF-LF 402
41 SMC_GPU_ISENSE
41 36 33 21 SMC_ADAPTER_EN R5085 10K 5% 1/16W MF-LF 402
41 SMC_CASE_OPEN R5086 10K 5% 1/16W MF-LF 402
41 SMC_EXCARD_CP R5088 10K 5% 1/16W MF-LF 402
41 PM_SLP_S5_L R5090 22K 5% 1/16W MF-LF 402
64 41 21 PM_SLP_S4_L
NEED TO TUNE VALUE FOR POWER SAVING
42 8 =PP3V3_S0_SMC
41 SMC_PA5 R5089 10K 5% 1/16W MF-LF 402

SMC Support

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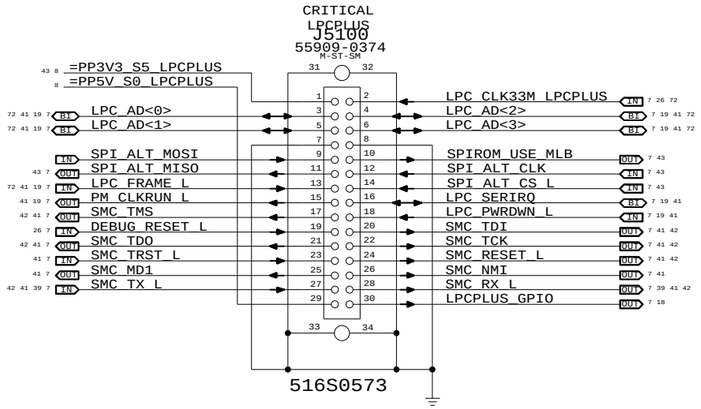
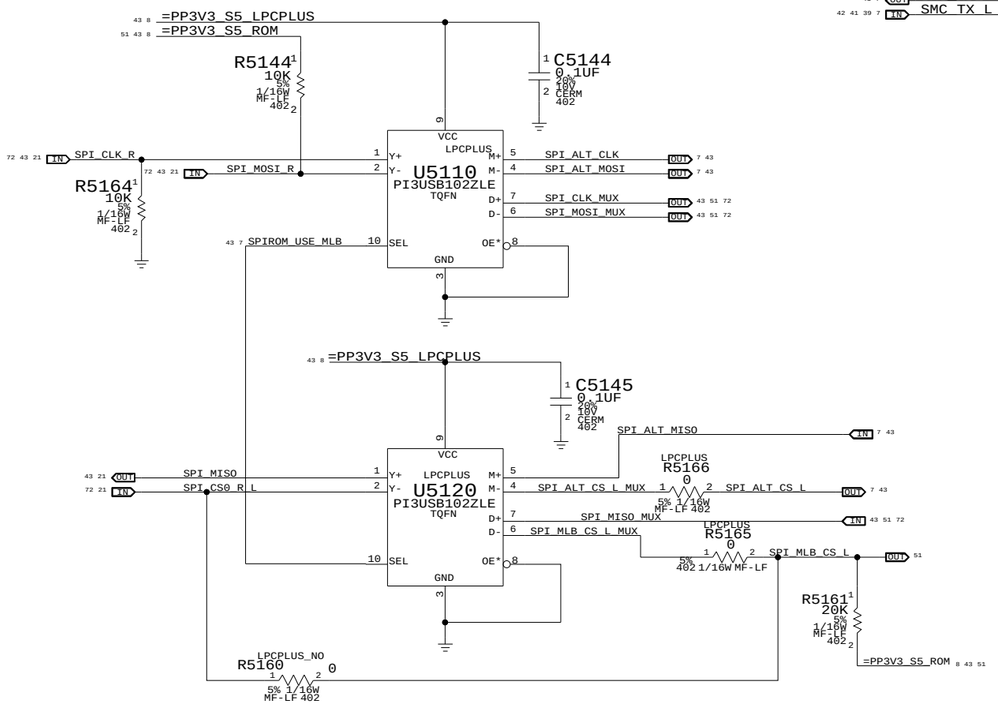
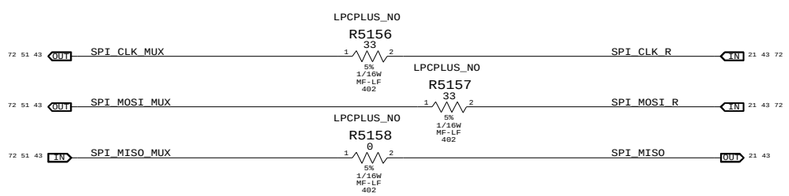
LPC+SPI Connector

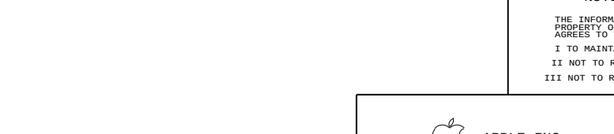


Alternate SPI ROM Support



SPI Bus Series Resistance Option





LPC+SPI Debug Connector

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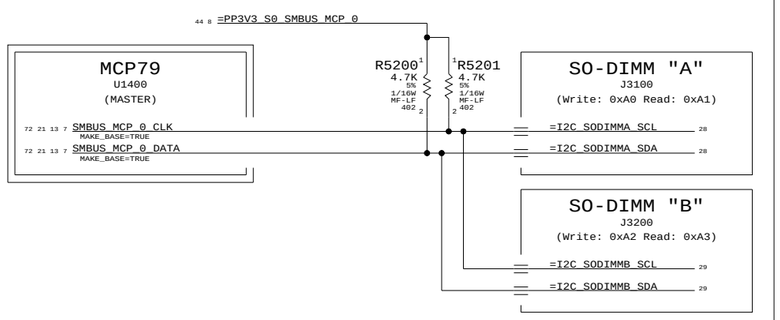
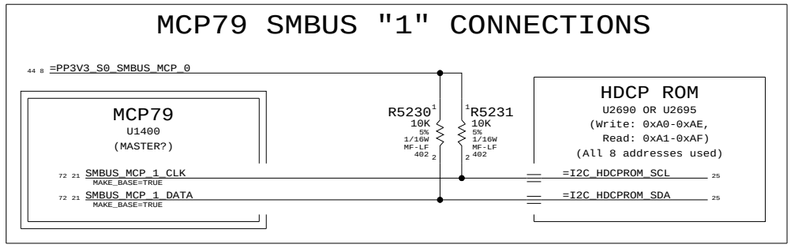
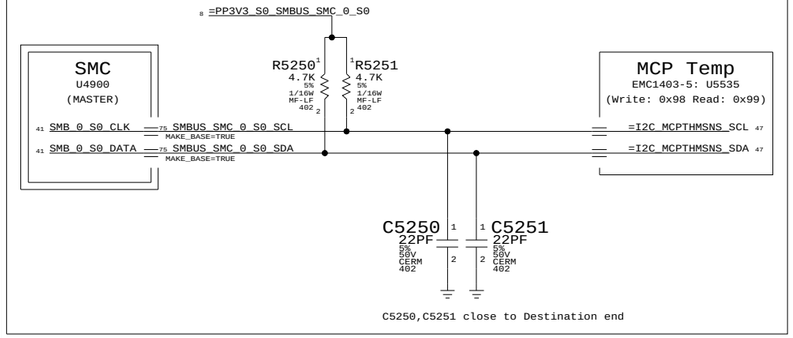
MCP79 SMBUS "0" CONNECTIONS



MCP79 SMBUS "1" CONNECTIONS



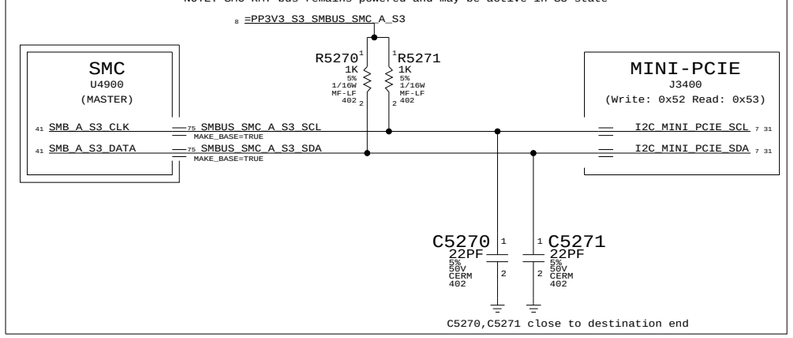
SMC "0" SMBus Connections



C5250,C5251 close to Destination end

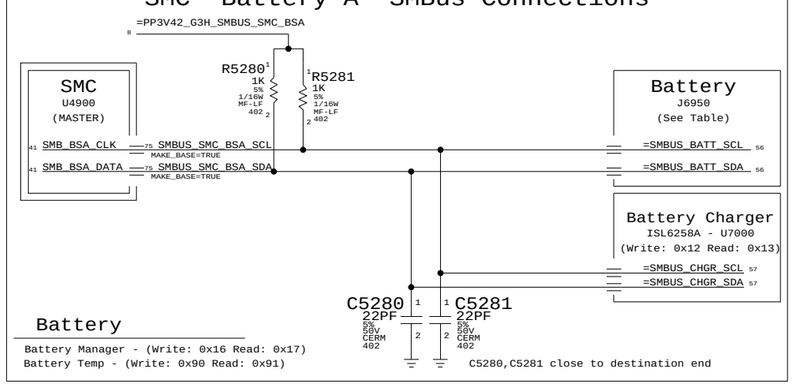
SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



C5270,C5271 close to destination end

SMC "Battery A" SMBus Connections

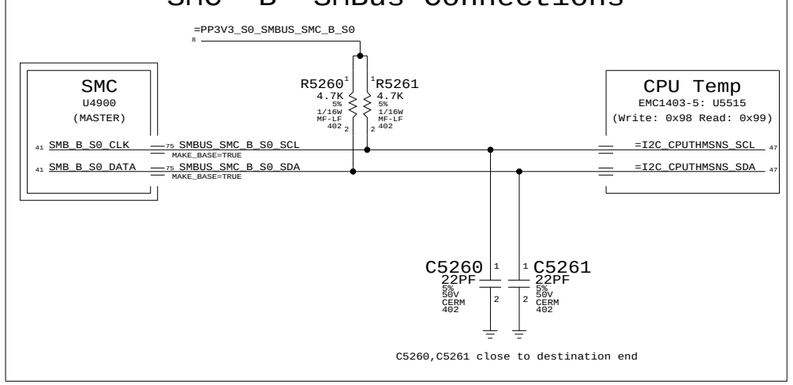


Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery Temp - (Write: 0x90 Read: 0x91)

C5280,C5281 close to destination end

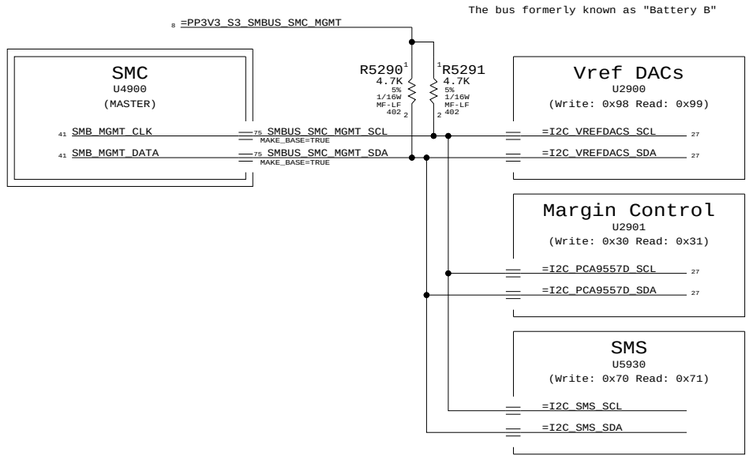
SMC "B" SMBus Connections



C5260,C5261 close to destination end

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



SMBUS CONNECTIONS

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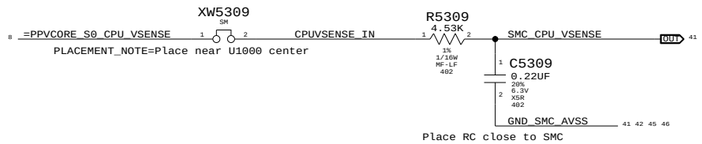
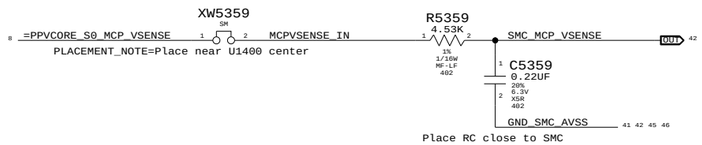
CPU Voltage Sense / Filter



PLACEMENT_NOTE=Place near U1000 center

Place RC close to SMC

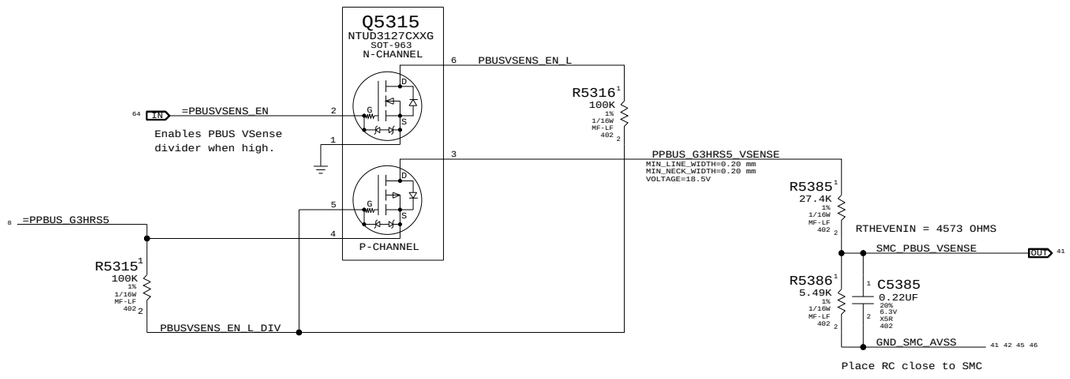
MCP Voltage Sense / Filter



PLACEMENT_NOTE=Place near U1400 center

Place RC close to SMC

PBUS VOLTAGE SENSE ENABLE & FILTER



Place RC close to SMC

VOLTAGE SENSING

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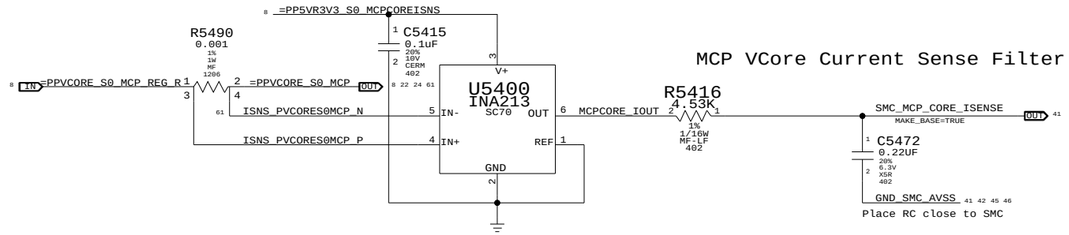
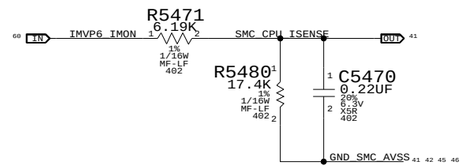
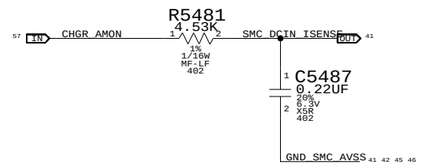
MCP VCore Current Sense



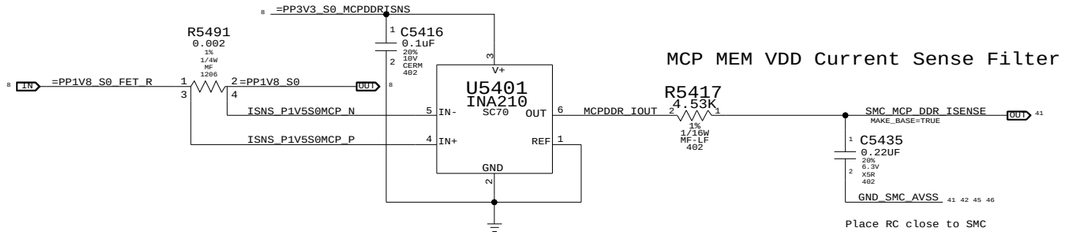
CPU VCORE LOAD SIDE CURRENT SENSOR / FILTER



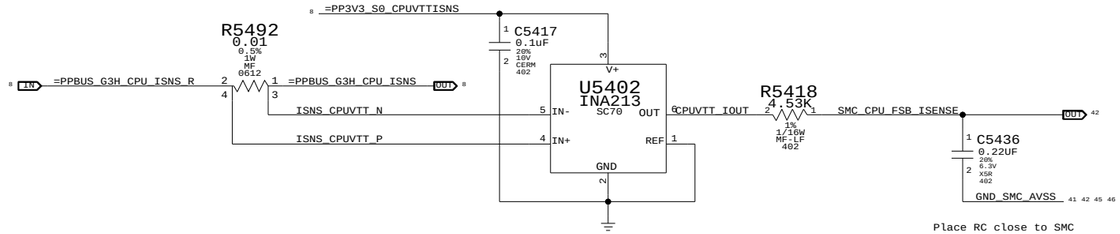
DC-IN (AMON) CURRENT SENSE



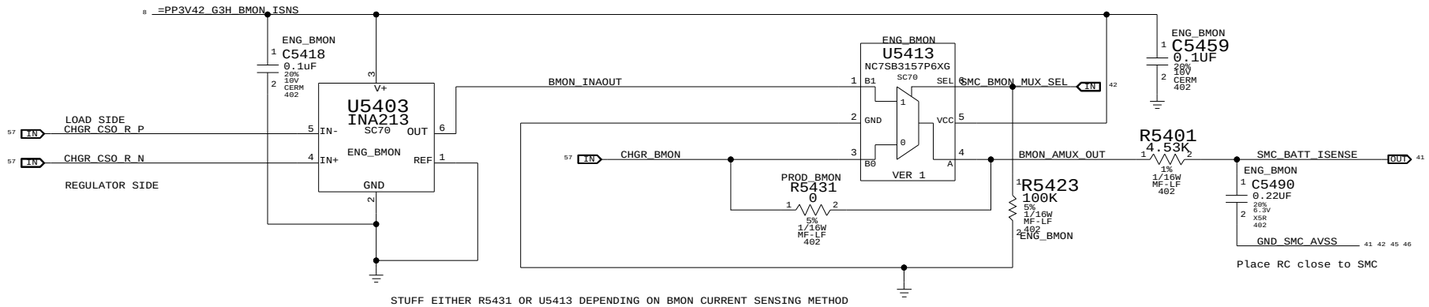
MCP MEM VDD Current Sense



CPU 1.05V CURRENT SENSE



CHARGER BMON CURRENT SENSE



STUFF EITHER R5431 OR U5413 DEPENDING ON BMON CURRENT SENSING METHOD

Current Sensing

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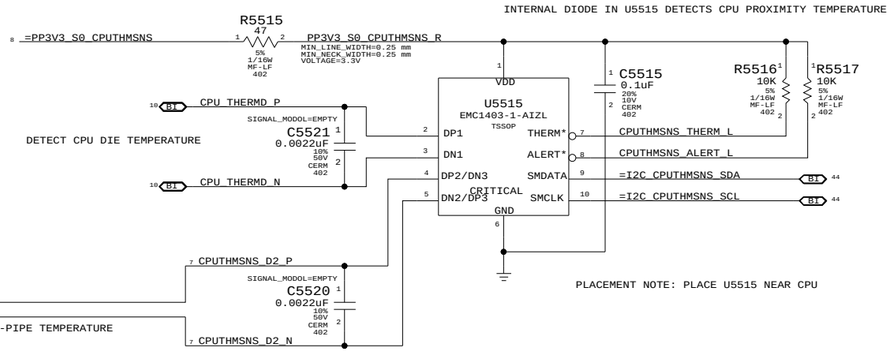
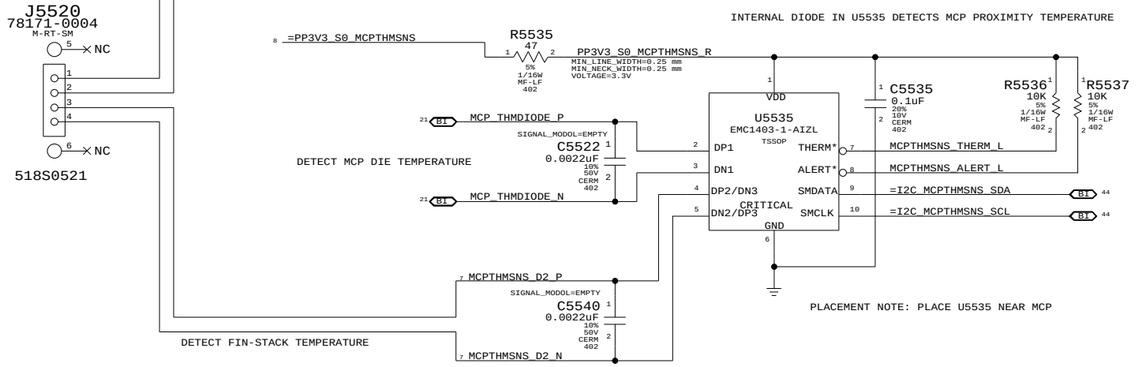
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



Thermal Sensors

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NONE	55	109

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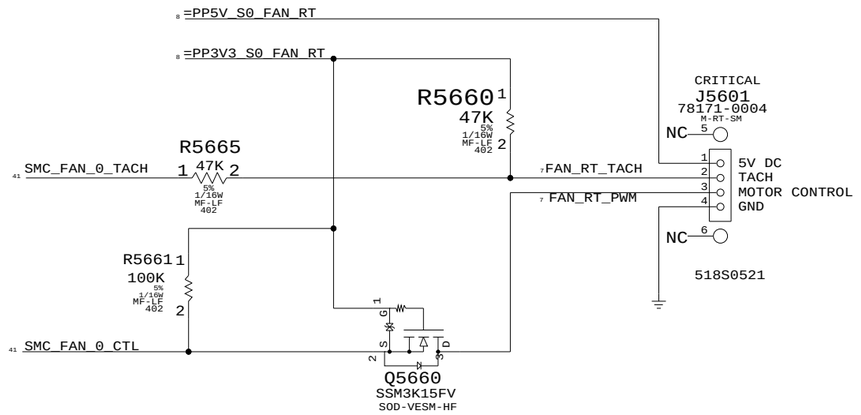

Fan

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8089	02

SCALE	SHT	OF
NONE	56	109

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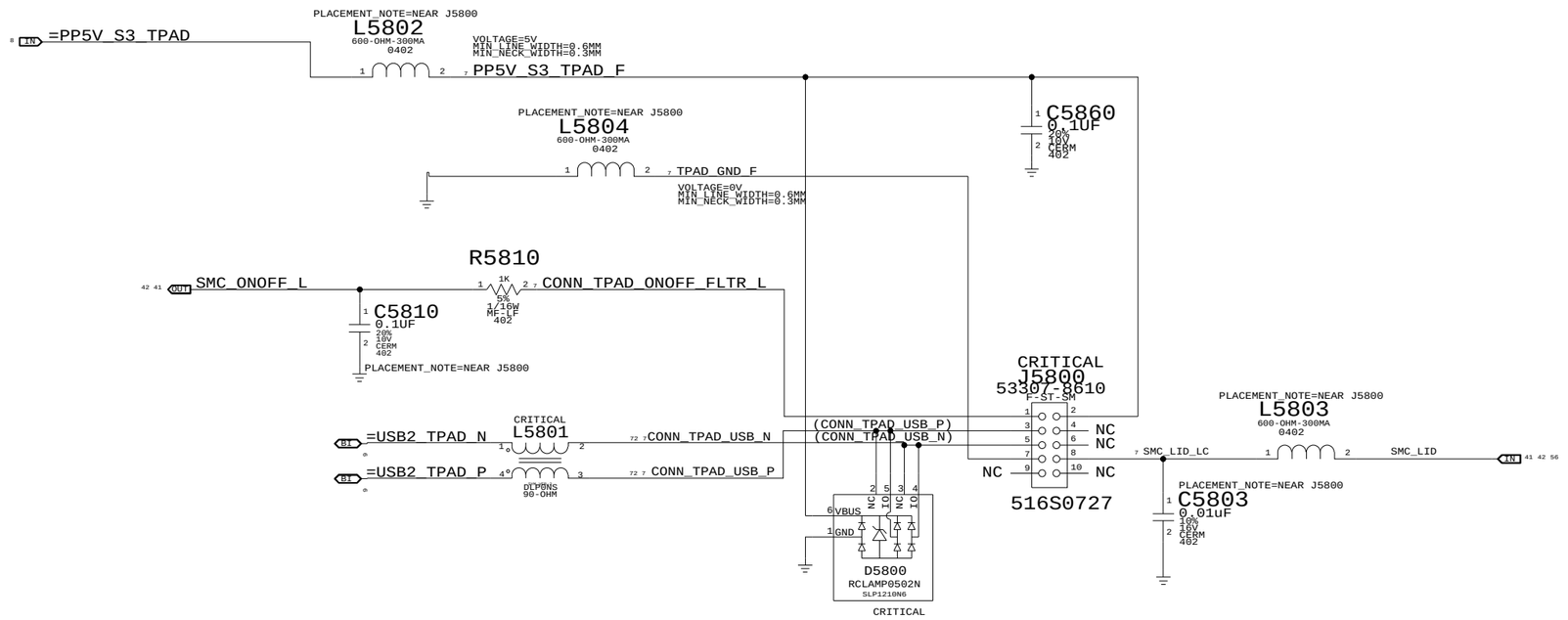
- SYNC WITH T18
- COPY THIS PAGE FROM T18 CSA.58

PLACEMENT NOTE

PLACE L5800,L5801,L5803 NEAR J5800
PLACE C5800,C5810,C5803 NEAR J5800
PLACE D5800 NEAR J5800

GEYSER



PLACE D5800 CLOSE J5800

GEYSER	
SYNC_MASTER=K36B_MLB	SYNC_DATE=08/17/2008

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APPLE INC.	SIZE D	DRAWING NUMBER 051-8089	REV. 02
	SCALE NONE	SHT 58 OF 109	

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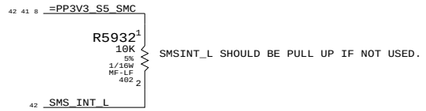
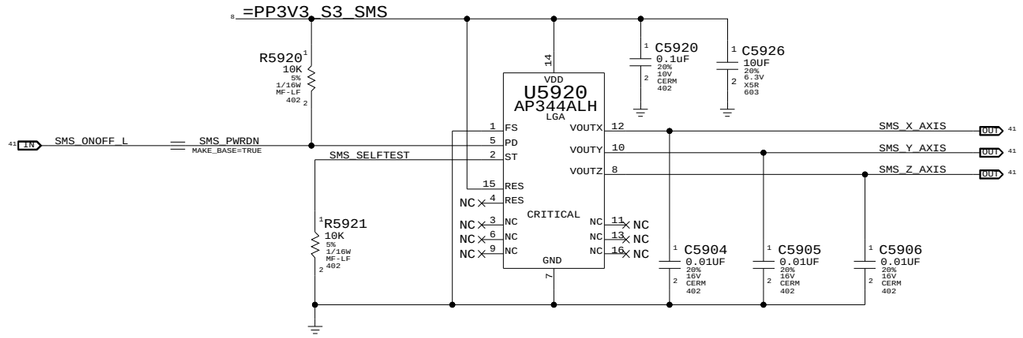
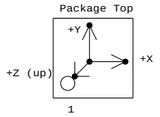


ANALOG SMS

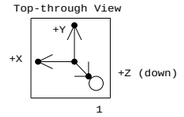


Desired orientation when placed on board top-side:



Front of system

Desired orientation when placed on board bottom-side:



SMS

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8089	02
SCALE	SHT	OF
NONE	59	109

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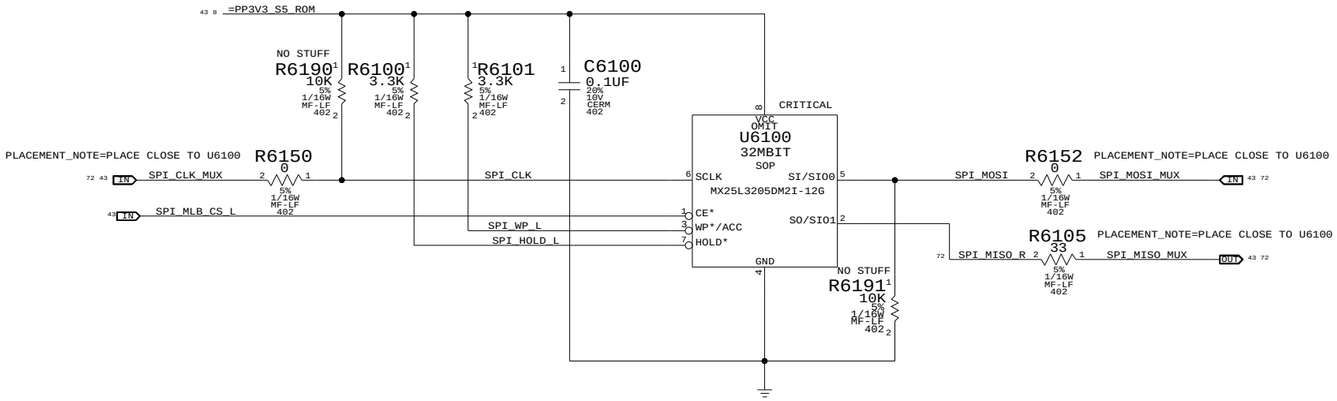

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHZ IS SECLECTED WITH R5164 AND R5144
ANY FO THE 4 FREQUENCIES CAN BE SELECTED
WITH R6190, R6191, R5164 AND R5144

SPI ROM

SYNC_MASTER=K36B_MLB SYNC_DATE=081/17/2008

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D	051-8089	02

SCALE NONE SHT 61 OF 109

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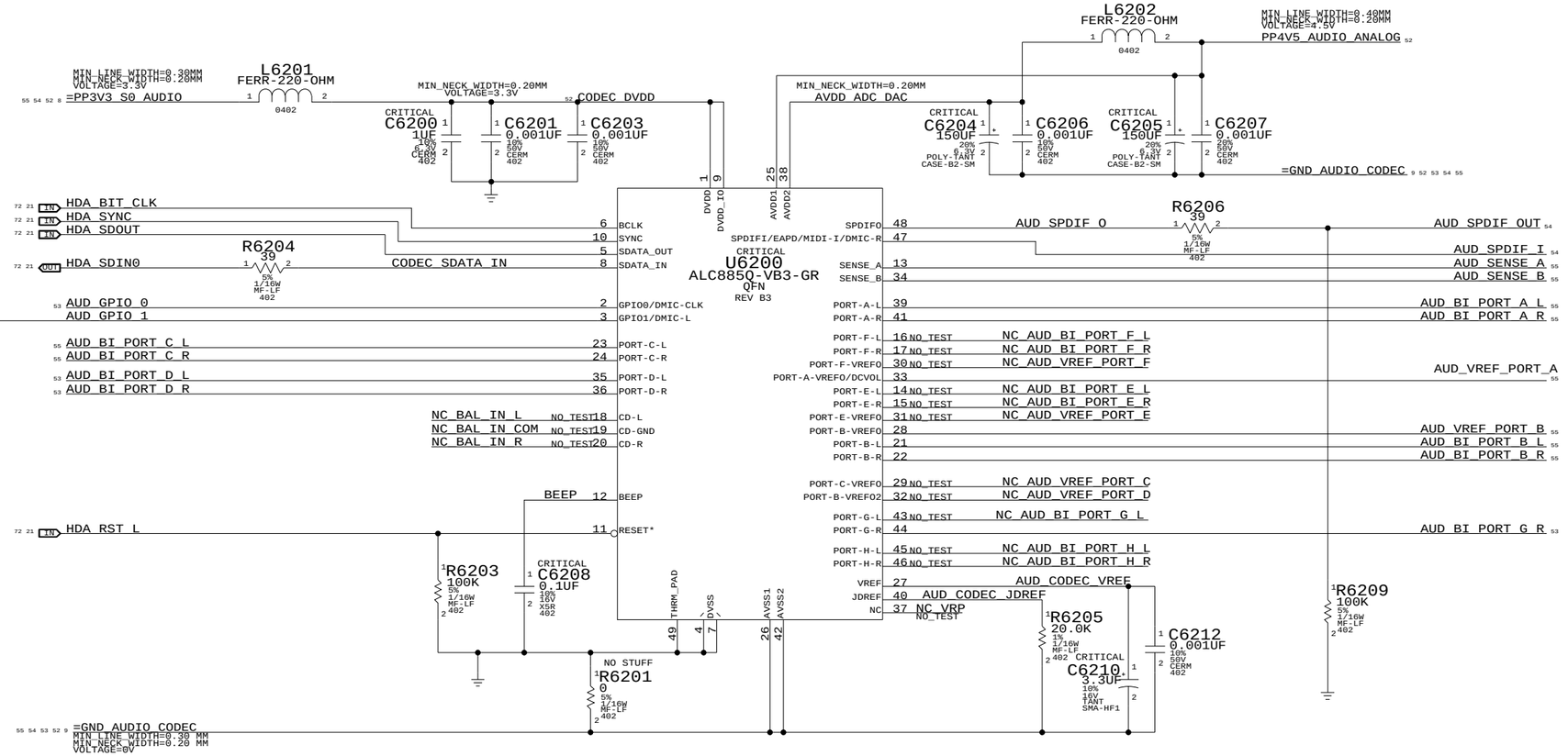
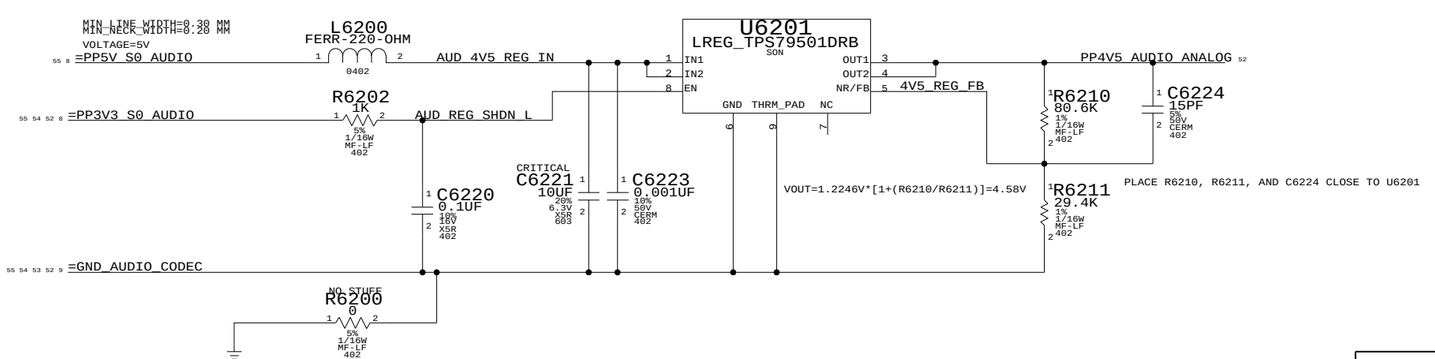
AUDIO CODEC

APPLE P/N 353S1538



AUDIO 4.5V REGULATOR

APPLE P/N 353S1576



AUDIO: CODEC

SYNC_MASTER=K36A_MLB

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SCALE: NONE	SHT 62 OF 109	

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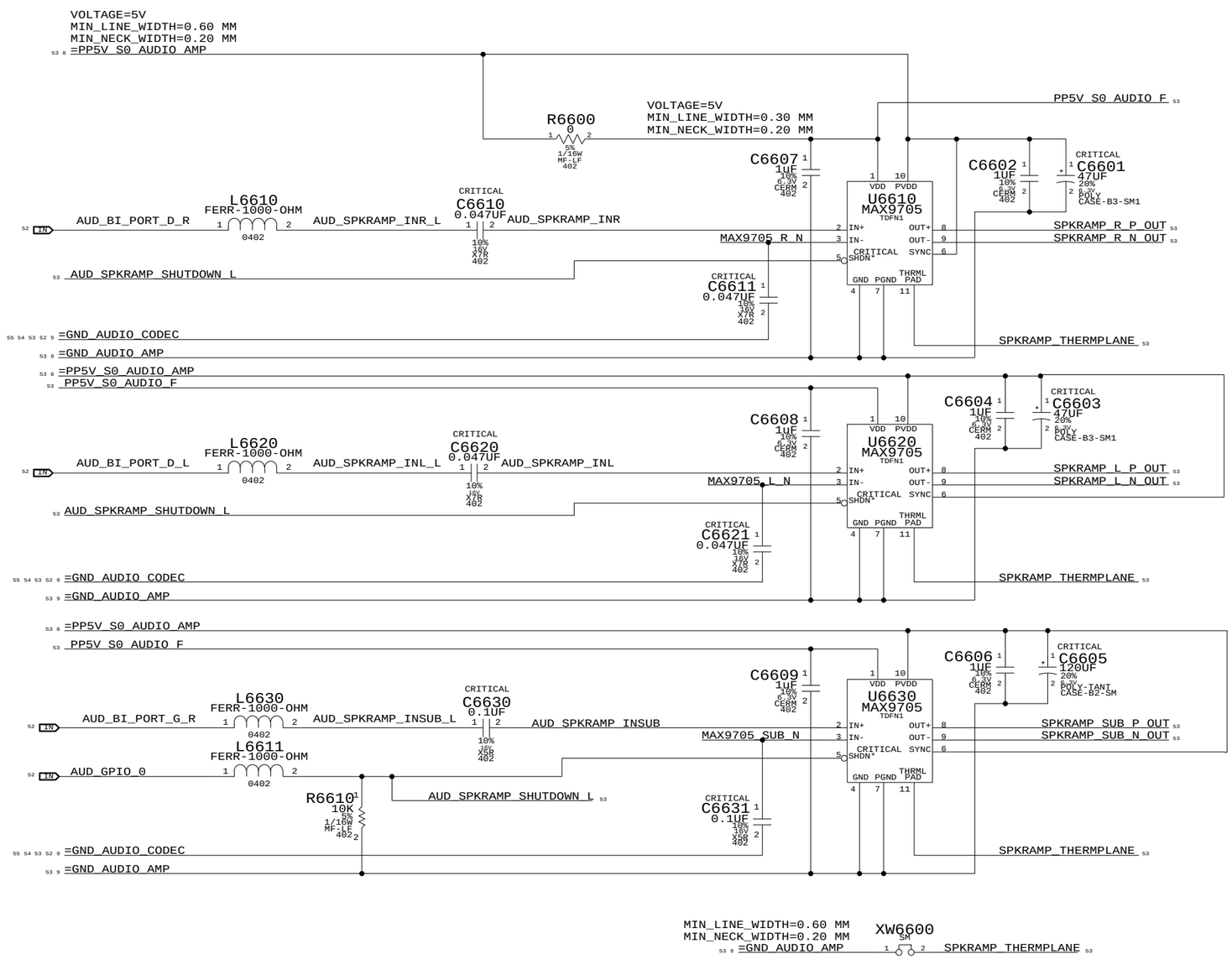
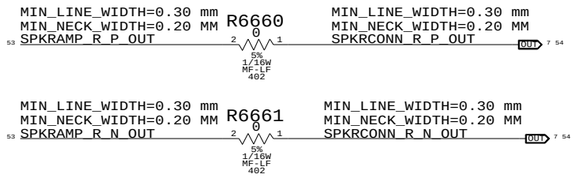
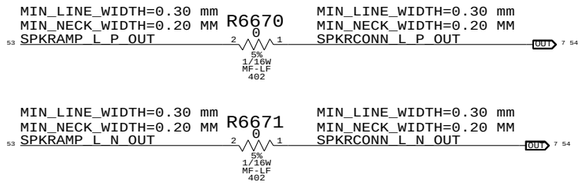
SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	12DB

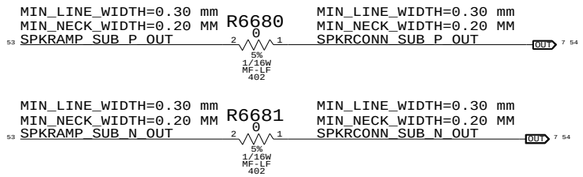




RIGHT SATELLITE



LEFT SATELLITE



SUB-TWEETER

AUDIO: SPEAKER AMP

SYNC_MASTER=K36A_MLB SYNC_DATE=08/29/2008

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D	051-8089	02
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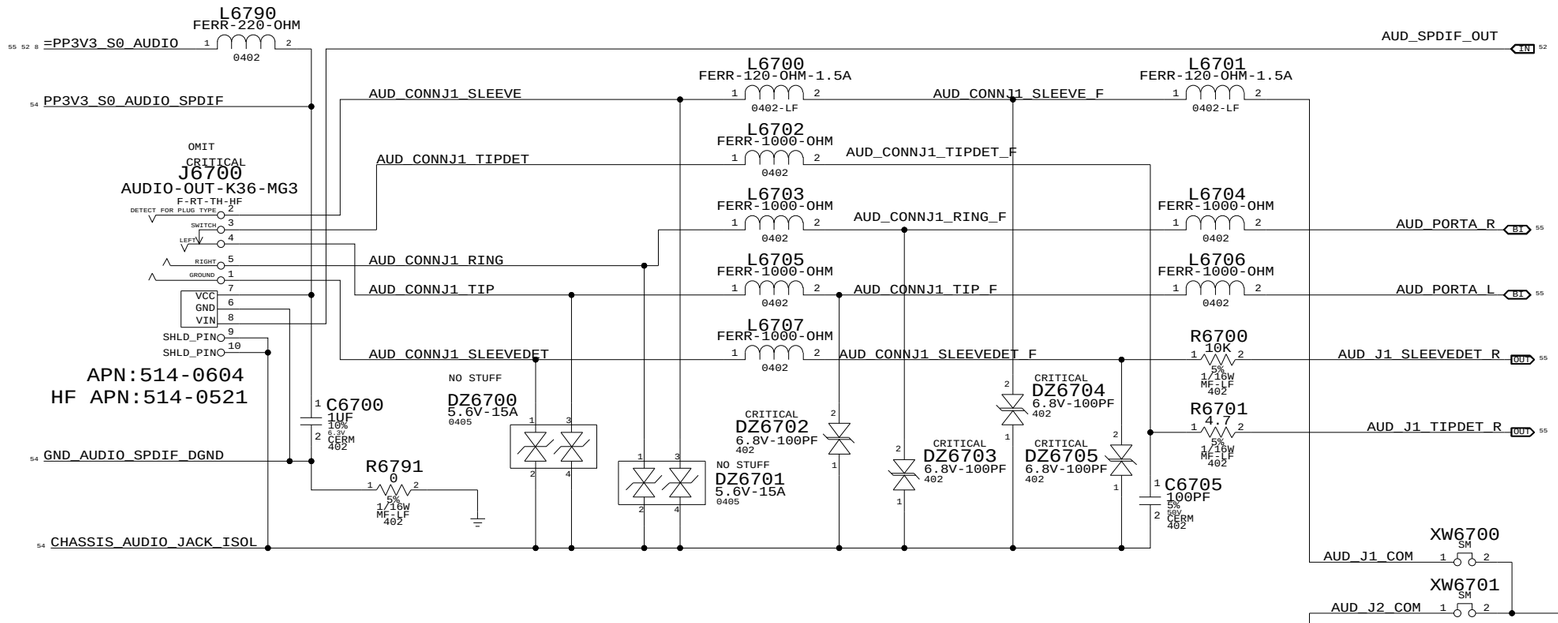
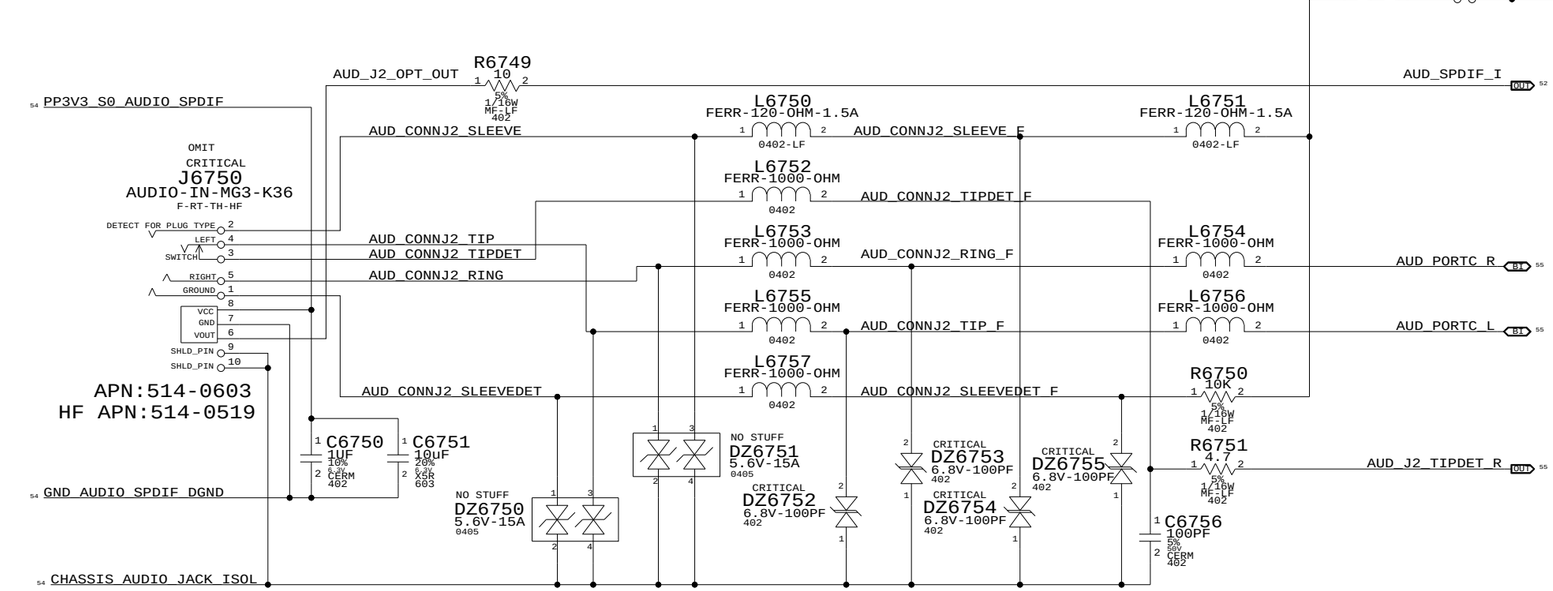
AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

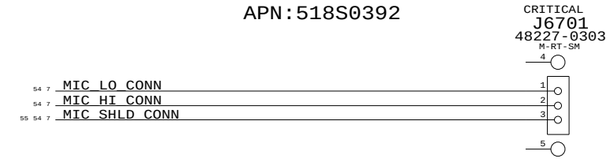


AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX



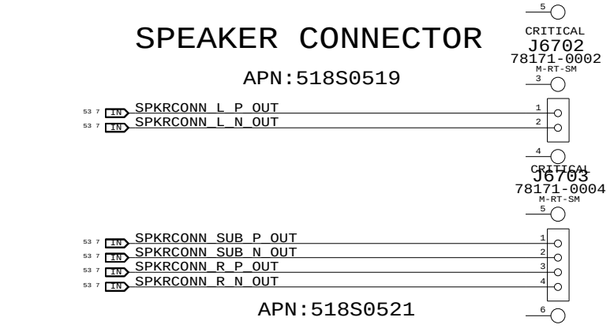
MIC CONNECTOR

APN:518S0392



SPEAKER CONNECTOR

APN:518S0519

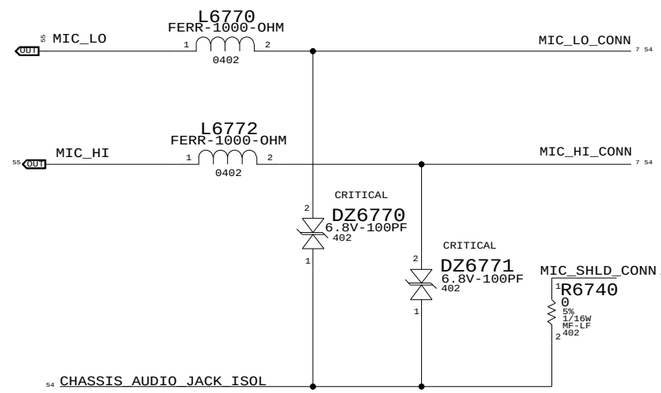


APN:518S0521

XW6705

=GND_CHASSIS_AUDIO_JACK — SM — CHASSIS_AUDIO_JACK_ISOL

MIC EMI FILTER



AUDIO: JACK

SYNC_MASTER=K36A_MLB SYNC_DATE=08/29/2008

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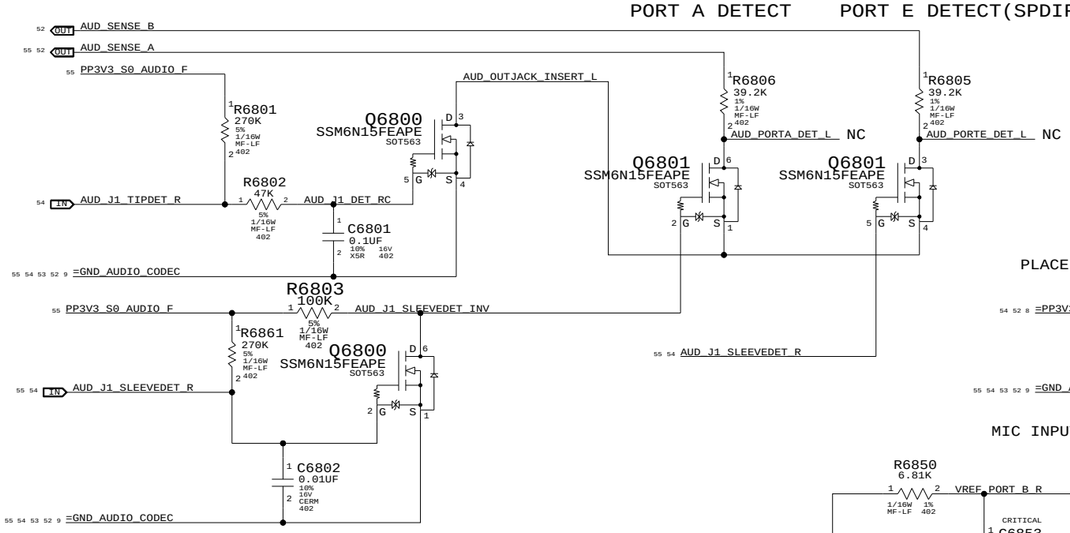
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0F (15)	0X05 (5)	0X15 (21,PORTA)	VREF_A(100%)	0X15 (21,PORTA)
SAT SPKR	0X26 (38)	0X25 (37)	0X14 (20,PORTD)	GPIO 0	N/A
SUB SPKR	0X0E (14)	0X04 (4)	0X16 (22,PORTG)	GPIO 0	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X1B (27,PORTE)

CODEC INPUT SIGNAL PATHS

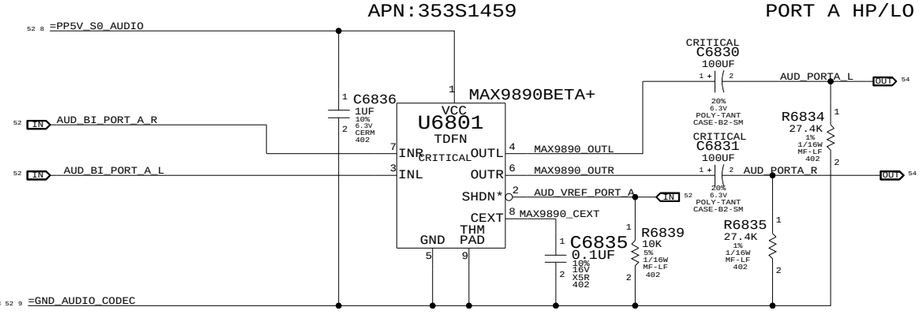
FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X1A (26,PORTC)	N/A	0X1A (26,PORTC)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X18 (24,PORTB)	VREF_B (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A

PORT A DETECT PORT E DETECT(SPDIF DELEGATE)

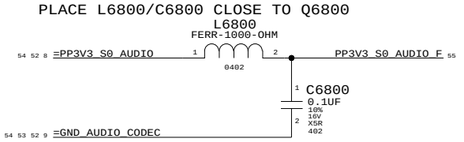


HP/LO DE-POP SWITCH
APN:353S1459

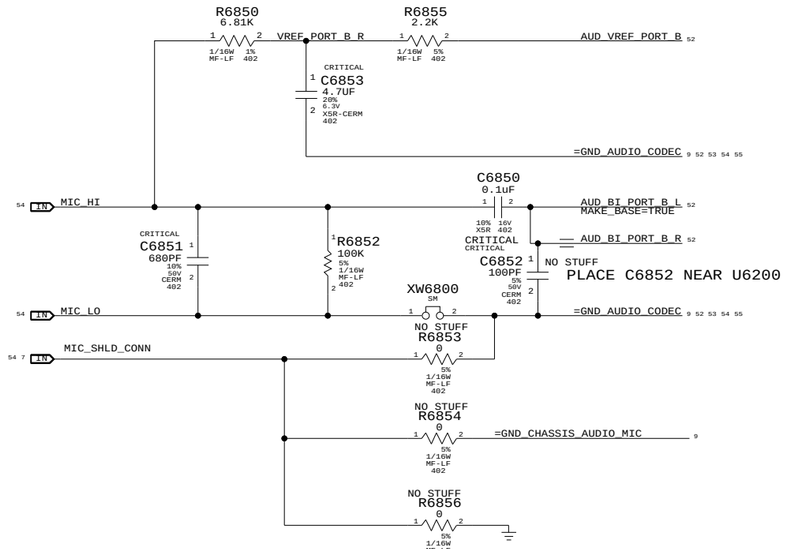
PORT A HP/LO



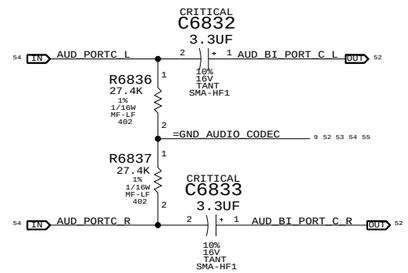
PLACE L6800/C6800 CLOSE TO Q6800



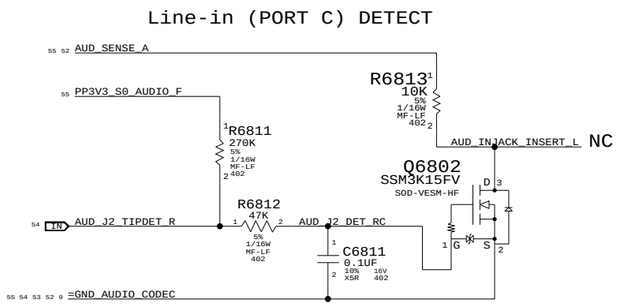
MIC INPUT CIRCUITRY



PORT C LI



Line-in (PORT C) DETECT



AUDIO: JACK TRANSLATORS

SYNC_MASTER=K36A_MLB SYNC_DATE=08/29/2008

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SCALE: NONE	SHT 68 OF 109	

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- DO WE NEED TO CHANGE BATTERY CONNECTOR?

MagSafe DC Power Jack

CRITICAL
J6900
78048-0573
M-RT-SM

518S0656

7 PP18V5_DCIN_FUSE
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V

7 ADAPTER_SENSE — R6928 0 5% 1/16W MF-LF 402

ADAPTER_SENSE_R

C6905 0.01UF 20% 50V CERM 603

CRITICAL
F6905
6AMP-24V
1206

Q6910 restricts system load to 10K-70K window until adapter detects system and enables 16.5V output.

=PP18V5_DCIN_CONN 8 56

1-Wire OverVoltage Protection

C6915 0.1UF 10% 25V X5R 402

<Ra> R6913 100K 5% 1/16W MF-LF 402
<Rb> R6914 100K 5% 1/16W MF-LF 402
<Vth>

ONEWIRE_DCIN_DIV
ONEWIRE_ESD

CRITICAL
U6915
LM397
SOT23-5-HF
ONEWIRE_OVERVOLT

If ADAPTER_SENSE > Vth
then turn off FET

Vth = Vdcin * (Rb / (Ra + Rb))
Vth = Vdcin / 2

R6920 24.3K 1% 1/16W MF-LF 402

PP18V5_DCIN_ONEWIRE
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V

R6915 270K 5% 1/16W MF-LF 402
R6916 270K 5% 1/16W MF-LF 402
R6917 270K 5% 1/16W MF-LF 402
R6918 270K 5% 1/16W MF-LF 402

ONEWIRE_EN

CRITICAL
Q6915
SSM3K15FV
SOD-VESM-HF

C6917 0.001UF 10% 50V CERM 402

VOLTAGE DIVIDER FROM DCIN ENSURES Q6910
Vgs is met when SYS_ONEWIRE is high or low.
Q6920 used as bilateral switch to ensure
SYS_ONEWIRE doesn't drive unpowered U6990

CRITICAL
Q6910
NTUD3127CXXG
SOT-963
P-CHN
Vgs(max) = 8V

R6911 180K 5% 1/16W MF-LF 402
R6912 470K 5% 1/16W MF-LF 402

ONEWIRE_PWR_EN_L_DIV
Vgs = 7.30V @ 20V DCIN
Vgs = 4.74V @ 13V DCIN

ONEWIRE_PWR_EN_L

CRITICAL
Q6910
NTUD3127CXXG
SOT-963
N-CHN

R6910 1K 5% 1/16W MF-LF 402
C6910 0.001UF 10% 50V CERM 402

SMC_BC_ACOK_RC
SMC_BC_ACOK 41 42 57

CRITICAL
Q6920
SSM6N15FEAPE
SOT563

SYS_ONEWIRE_BILAT
SYS_ONEWIRE BI 41 42

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

=PP18V5_DCIN_CONN 56 8
R6905 47 5% 1/8W MF-LF 805
PPDCIN_S5_P3V42G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=18.5V

BATT_POS_F 57 56
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=12.6V

D6905
HN2D01JEAPE
SOT665
NC — NC

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

P3V42G3H_BOOST

C6990 10uF 10% 25V X5R 1206-1

U6990
LT3470ETS8
TSOT23-8
VIN BOOST SHDN* SW BIAS NC CRITICAL FB GND

C6994 0.22uF 20% 6.3V X5R 402

CRITICAL
L6995
33UH
CDPH4D19FHF-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

=PP3V42_G3H_REG 8
Vout = 3.425V
200mA max output
(Switcher limit)

C6995 22pF 5% 50V CERM 402

<Ra> R6995 348K 1% 1/16W MF-LF 402
<Rb> R6996 200K 1% 1/16W MF-LF 402

C6999 22UF 20% 6.3V CERM 805

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

LID HALL EFFECT SENSOR

MLB TOP VIEW
PIN 1

BATTERY/LID CONNECTOR

CRITICAL
J6950
8199-3520-M281
F-ST-SM

APN:516S0620
HFAPN:516S0735

NC — VOID — NC

7 PPVBAT_G3H_CONN_F

7 SMBUS_BATT_SCL_F
7 SMBUS_BATT_SDA_F
7 SMC_BS_ALRT_L_F

CRITICAL
D6950
RCLAMP2402B
SC-79

L6901
FERR-50-OHM
SM-LF
BATT_POS_F 56 57

L6902
120-OHM-0.3A-EMI
0402-LF
=SMBUS_BATT_SCL 44

L6903
120-OHM-0.3A-EMI
0402-LF
=SMBUS_BATT_SDA 44

L6904
120-OHM-0.3A-EMI
0402-LF
SMC_BS_ALRT_L 41 42

L6909
600-OHM-300MA
0402
8 =PP3V42_G3H_LIDSWITCH
7 PP3V42_G3H_LIDSWITCH_F

L6907
600-OHM-300MA
0402
7 GND_SMC_LID_F

L6908
600-OHM-300MA
0402
49 42 41 SMC_LID
7 SMC_LID_F

C6920 0.01uF 10% 16V CERM 402
C6921 0.01uF 10% 16V CERM 402
=GND_BATT_CHGND 9 56

C6942 0.001UF 10% 50V CERM 402
C6943 0.001UF 10% 50V CERM 402
C6944 47pF 5% 50V CERM 402
C6945 47pF 5% 50V CERM 402

56 9 =GND_BATT_CHGND

DC-In & Battery Connectors

SYNC_MASTER=RAYMOND
SYNC_DATE=08/17/2008

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PBUS SUPPLY / BATTERY CHARGER

=PP18V5_G3H_CHGR
D7010 1SS418 SOD-723-HF
C7063 0.1UF 10% 16V X5R 402
R7098 100K 5% 1/10W MF-LF 402
Q7000 HAT1127H LFPAK-SR CRITICAL
PPVDCIN_G3H_PRE2
Q7001 HAT1127H LFPAK-SR CRITICAL
PPVDCIN_G3H_PRE
R7099 100K 5% 1/10W MF-LF 402
CHGR_LOWCURRENT_GATE_MOS
R7062 62K 5% 1/10W MF-LF 402
CHGR_DCIN
R7010 30.1K 1% 1/16W MF-LF 402
CHGR_SGATE
R7001 62K 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
=PP3V42_G3H_CHGR
R7060 57.6K 1% 1/10W MF-LF 402
C7060 0.1UF 10% 16V X5R 402
CHGR_AMON
R7061 1.82K 1% 1/16W MF-LF 402
CHGR_LOWCURRENT_REF
U7060 CRITICAL TL331 SOT23-5
CHGR_LOWCURRENT_GATE
(CHGR_ACIN)
C7010 0.1UF 10% 25V X5R 402
R7011 9.31K 1% 1/16W MF-LF 402
CHGR_VDD
R7040 4.7 5% 1/16W MF-LF 402
CHGR_VDDP
C7041 1UF 10% 16V X5R 402-1
C7040 1UF 10% 16V X5R 402-1
C7047 1UF 10% 16V X5R 402-1
=PP3V42_G3H_CHGR
R7023 10 5% 1/10W MF-LF 402
CHGR_CSIP_XW7020
XW7020 SM
C7024 0.047UF 10% 16V CERM 402
R7021 10 5% 1/16W MF-LF 402
XW7021 SM
CHGR_CSIN_XW7021
R7020 0.02 0.5% 1W MF 0612 CRITICAL
PP18V5_S5_CHGR_SW_R
C7020 22UF 20% 25V POLY-TANT CASE-D2-SM CRITICAL
C7021 22UF 20% 25V POLY-TANT CASE-D2-SM CRITICAL
C7022 1UF 10% 25V X5R 603-1
C7023 1UF 10% 25V X5R 603-1
C7027 0.001UF 10% 50V CERM 402
CHGR_SCL
CHGR_SDA
U7000 CRITICAL ISL6258A QFN
VHST SCL SDA VREF ACIN ICOMP VCOMP VNEG CSOP CSON THRM_PAD AGND PGND VDD VDDP AGATE CSIP CSIN BGATE DCIN BOOT UGATE PHASE LGATE TRKL* NC AMON BMON ACOK
CHGR_AGATE
CHGR_CSIP
CHGR_CSIN
CHGR_BGATE
CHGR_DCIN
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
CHGR_AMON
CHGR_BMON
CHGR_ACOK
C7061 0.1UF 10% 25V X5R 402
C7062 0.1UF 10% 25V X5R 402
GND_CHGR_SGND
Q7020 RJK0305DPB LFPAK-HF CRITICAL
C7025 0.1UF 10% 25V X5R 402
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
L7000 4.7UH-9.5A IHLP4040DZ-SM CRITICAL
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
PPVBAT_G3H_CHGR_REG
R7008 0.01 0.5% 1W MF 0612
PPVBAT_G3H_CHGR_OUT
F7000 7AMP 1206 CRITICAL
=PPBUS_G3H
TO SYSTEM
MAX CURRENT = 7A
PWM FREQ. = 400 KHZ
C7008 33UF 20% 16V POLY-TANT CASED2E-SM CRITICAL
C7011 1UF 10% 25V X5R 603-1
C7028 0.001UF 10% 50V CERM 402
PWM FREQ. = 400KHZ
MAX CURRENT = 7 A
(??? LIMITED)
R7090 2.2 5% 1/16W MF-LF 402 NO STUFF
EMI request
CHGR_PHASE_SNUBBER
C7090 100PF 5% 50V CERM 402 NO STUFF
EMI request
Q7021 RJK0305DPB LFPAK-HF CRITICAL
R7031 10 5% 1/16W MF-LF 402
CHGR_CSO_R_P
R7047 10 5% 1/16W MF-LF 402
CHGR_CSO_R_N
C7044 0.01UF 10% 16V CERM 402
C7042 0.033UF 10% 16V X5R 402
R7045 56.2K 1% 1/16W MF-LF 402
CHGR_VCOMP_R
C7043 0.1UF 10% 16V X5R 402
C7045 0.001UF 10% 50V CERM 402
R7046 3.01K 1% 1/16W MF-LF 402
CHGR_VNEG_R
C7046 470PF 10% 50V CERM 402
XW7000 SM
C7026 0.001UF 10% 50V X7R 402
GND_CHGR_SGND
GND CHGR SGND
(CHGR_CSOP)
(CHGR_CSON)
(CHGR_CSO_R_N)
AMON PULLDOWN LOGIC

=SMBUS_CHGR_SCL — CHGR_SCL
=SMBUS_CHGR_SDA — CHGR_SDA
ACOK pullup/down on SMC page
SMC_BC_ACOK — CHGR_ACOK
MAKE_BASE=TRUE

BATTERY CHARGING

CHGR_AMON
=PP3V42_G3H_CHGR
R7074 1M 5% 1/16W MF-LF 402
Q7070 SSM6N15FEAPE SOT563
NO STUFF
R7075 1M 5% 1/16W MF-LF 402
CHGR_VDD_L
Q7070 SSM6N15FEAPE SOT563
CHGR_VDD
R7073 1K 5% 1/16W MF-LF 402
CHGR_VDD_R

PPVBAT_G3H_CHGR_OUT
C7050 0.01UF 10% 16V CERM 402
C7051 0.1UF 10% 16V X5R 402
Q7050 FDS6681Z SO-8 CRITICAL
BATT_POS_INRUSH
Q7052 FDS6681Z SO-8 CRITICAL
TO BATTERY
BATT_POS_F
CHGR_BGATE
C7052 0.1UF 10% 16V X5R 402
BATT_POS_GATE
R7052 1M 5% 1/16W MF-LF 402
R7053 330K 5% 1/16W MF-LF 402

PBUS Supply/Battery Charger
SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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D	051-8089	02
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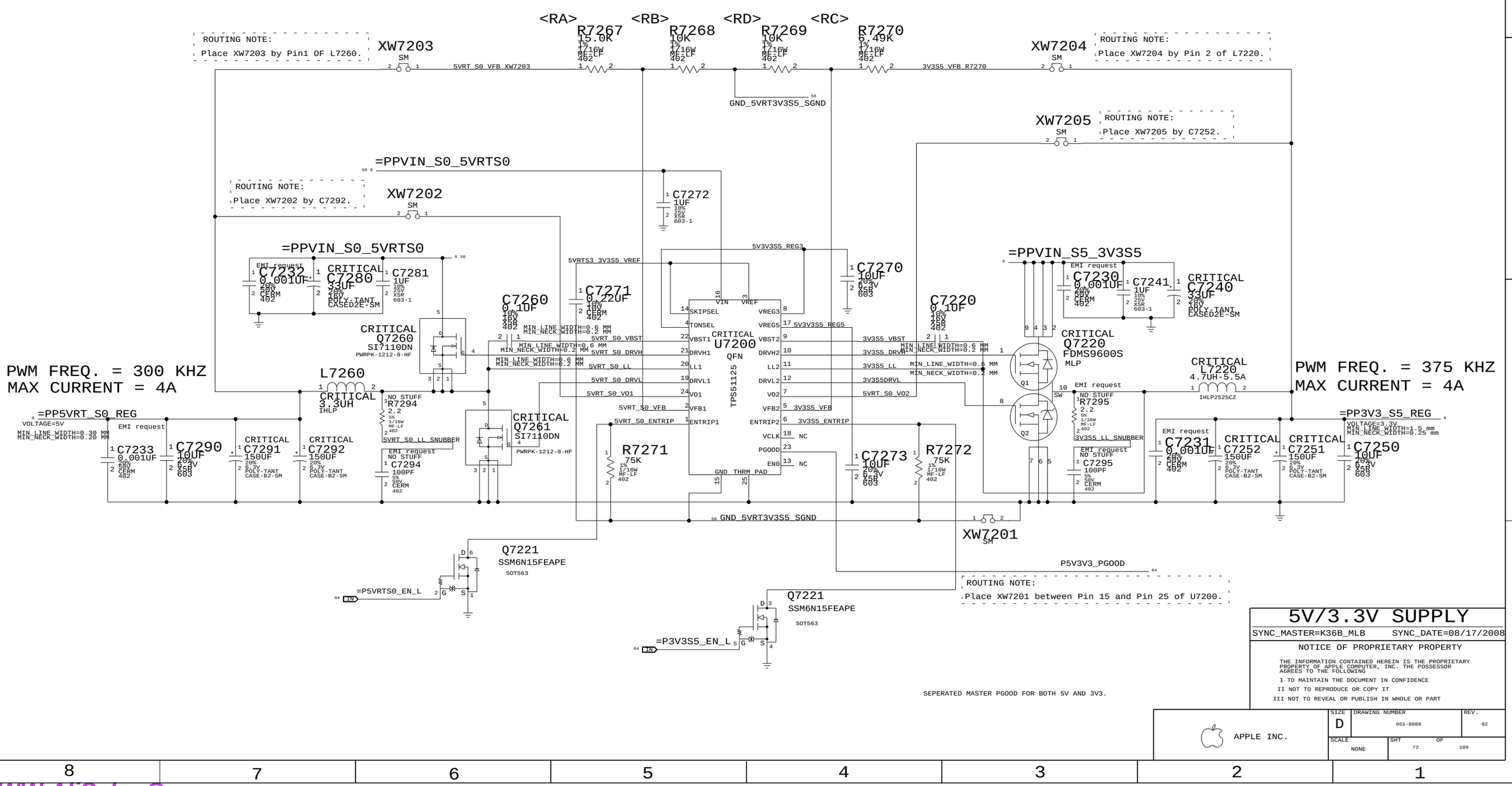
5V_RT/3.3V POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



5V/3.3V SUPPLY

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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SCALE	SHT	OF
NONE	72	109

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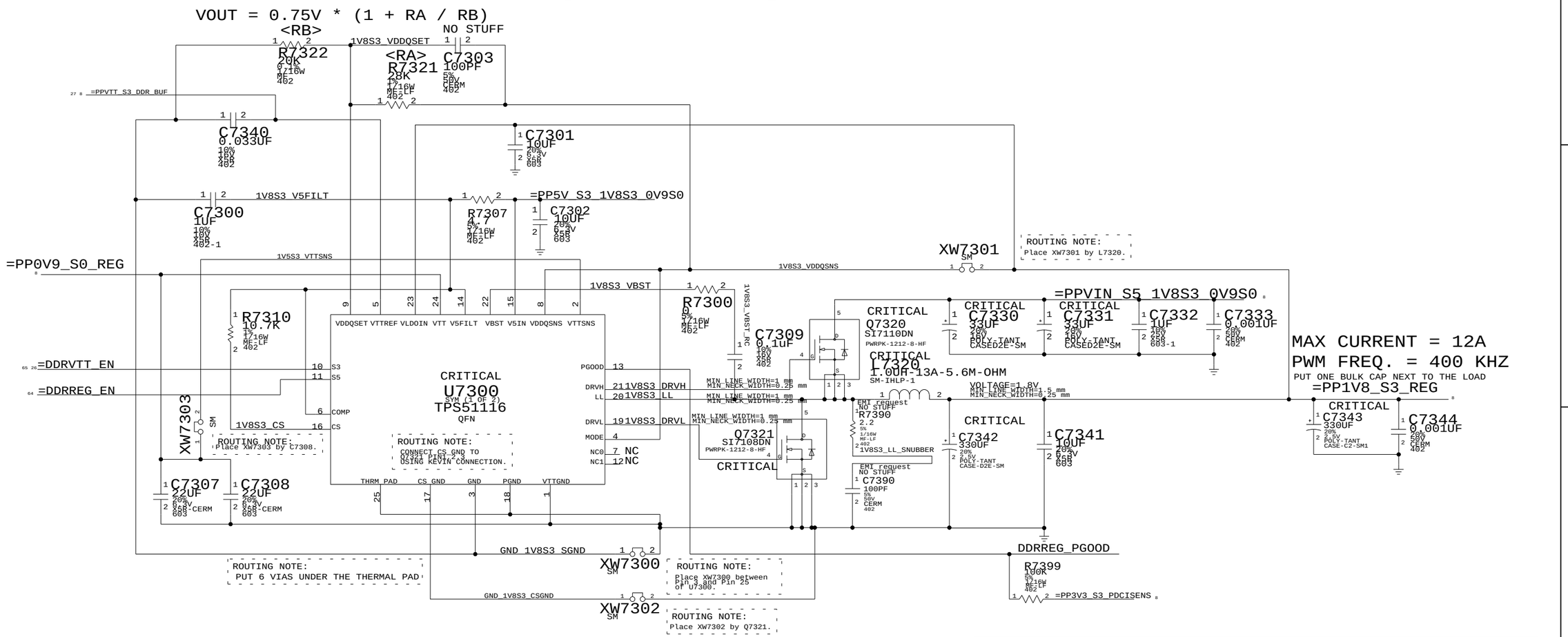
1.8V/0.9V(DDR2) POWER SUPPLY


VOUT = 0.75V * (1 + RA / RB)
<RB>
R7322 20K 1% 1/16W MF 402
<RA>
R7321 28K 1% 1/16W MF-LF 402
NO STUFF
C7303 100PF 5% 50V CERM 402
=PPVTT_S3_DDR_BUF
C7340 0.033UF 10% 16V X5R 402
C7301 10UF 20% 6.3V X5R 603
1V8S3_V5FILT
C7300 1UF 10% 10V X5R 402-1
=PP5V_S3_1V8S3_0V9S0
R7307 4.7 5% 1/16W MF-LF 402
C7302 10UF 20% 6.3V X5R 603
1V5S3_VTTSNS
1V8S3_VDDQSNS
XW7301 SM
ROUTING NOTE: Place XW7301 by L7320.
=PP0V9_S0_REG
1V8S3_VBST
R7300 0 5% 1/16W MF-LF 402
=PPVIN_S5_1V8S3_0V9S0
CRITICAL
Q7320 SI7110DN PWRPK-1212-8-HF
C7309 0.1UF 10% 10V X5R 402
C7330 33UF 20% 16V POLY-TANT CASED2E-SM
C7331 33UF 20% 16V POLY-TANT CASED2E-SM
C7332 1UF 10% 25V X5R 603-1
C7333 0.001UF 20% 50V CERM 402
L7320 1.0UH-13A-5.6M-OHM SM-IHLP-1
MAX CURRENT = 12A
PWM FREQ. = 400 KHZ
PUT ONE BULK CAP NEXT TO THE LOAD
=PP1V8_S3_REG
R7310 10.7K 1% 1/16W MF-LF 402
=DDRVTT_EN
=DDRREG_EN
U7300 SYM (1 OF 2) TPS51116 QFN
VDDQSET VTTREF VLDOIN VTT V5FILT VBST V5IN VDDQSNS VTTSNS
PGOOD DRVH LL DRVL MODE NC0 NC1
S3 S5 COMP CS
1V8S3_DRVH 1V8S3_LL 1V8S3_DRVL NC NC
MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.25 mm
EMI request NO STUFF R7390 2.2 5% 1/16W MF-LF 402 1V8S3_LL_SNUBBER
EMI request NO STUFF C7390 100PF 5% 50V CERM 402
Q7321 SI7108DN PWRPK-1212-8-HF
CRITICAL
C7342 330UF 20% 2V POLY-TANT CASE-D2E-SM
C7341 10UF 20% 6.3V X5R 603
C7343 330UF 20% 2.5V POLY-TANT CASE-C2-SM1
C7344 0.001UF 20% 50V CERM 402
XW7303 SM
1V8S3_CS
ROUTING NOTE: Place XW7303 by U7300.
ROUTING NOTE: CONNECT CS GND TO OUTPUT CAP'S GND USING KELVIN CONNECTION.
C7307 22UF 20% 6.3V X5R-CERM 603
C7308 22UF 20% 6.3V X5R-CERM 603
THRM PAD CS GND GND PGND VTTGND
GND_1V8S3_SGND
XW7300 SM
ROUTING NOTE: Place XW7300 between Pin 1 and Pin 25 of U7300.
ROUTING NOTE: PUT 6 VIAS UNDER THE THERMAL PAD
GND_1V8S3_CSGND
XW7302 SM
ROUTING NOTE: Place XW7302 by Q7321.
DDRREG_PGOOD
R7399 100K 5% 1/16W MF-LF 402
=PP3V3_S3_PDCISENS

STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

1.8V/0.9V DDR2 SUPPLY

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DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

PWM FREQ. = 300 KHZ
MAX CURRENT = 44A
LOAD LINE SLOPE = -2.1 MV/A

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

IMVP6 CPU VCORE REGULATOR

LATEST ISSUE: 2007/01/23

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P		
CPU_VCCSENSE_N		
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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- SYNC WITH T18
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MCP VCORE/5V_S3 LEFT REGULATOR

=PPVIN_S3_5VLTS3
8 VOLTAGE=12.6V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C7512 0.001UF 20% 50V CERM 402
Q7510 SI7110DN PWRPK-1212-8-HF
C7510 33UF 20% 16V POLY-TANT CASED2E-SM
C7511 1UF 10% 25V X5R 603-1
Q7511 SI7110DN PWRPK-1212-8-HF

(P5VLTS3_UGATE) MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM GATE_NODE=TRUE
(P5VLTS3_LGATE) MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM GATE_NODE=TRUE
(P5VLTS3_BOOT) MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C7514 0.1UF 10% 50V X7R 603-1 SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM (P5VLTS3_PHASE)

PP5V_S3_MCPREG_LDO
=PPVIN_S0_MCPREG_VIN
C7500 10UF 10% 25V X5R 805
C7501 1UF 10% 6.3V CERM 402

(Internal 10-ohm path from PVCC to VCC)
PP5V_S0_MCPREG_VCC MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=5V
MCPREG_VREF3
C7504 1UF 10% 6.3V CERM 402
C7503 1UF 10% 6.3V CERM 402
C7502 4.7UF 20% 6.3V X5R-CERM 402
Max load 100mA
PP5V_S3_MCPREG_LDO VOLTAGE=5V

TDP: 5.2A
(Q7510 LIMIT)
7A MAX OUTPUT
VOUT = 5V
FREQ = 400 KHZ
=PP5VLT_S3_REG

CRITICAL L7520 3.3UH IHLP
C7518 0.001UF 20% 50V CERM 402
C7517 150UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C7515 150UF 20% 6.3V POLY-TANT CASE-B2-SM
C7516 10UF 20% 10V X5R 805
(=PP5VLT_S3_REG)
XW7501 SM PLACEMENT_NOTE=Place next to C7516
P5VLTS3_VSNS
NO STUFF R7595 2.2 5% 1/16W MF-LF 402 EMI request
P5VLTS3_PHASE_SNUBBER
NO STUFF C7595 100PF 5% 50V CERM 402 EMI request
NO STUFF R7521 61.9K 1% 1/10W MF-LF 402 <Ra>
NO STUFF C7520 100PF 5% 50V CERM 402
R7522 0 5% 1/10W MF-LF 402 <Rb>
R7520 180K 5% 1/10W MF-LF 402
XW7500 SM
C7530 0.1UF 20% 10V CERM 402
R7530 180K 5% 1/10W MF-LF 402

U7500 QFN N08020431

6	VIN	LDO	7
17	VBST1	LDOREFIN	8
15	DRVH1	VBST2	24
16	LL1	DRVH2	26
18	DRVL1	LL2	25
10	VOUT1	DRVL2	23
14	EN1	VOUT2	30
9	VSW	EN2	27
11	VFB1	REFIN2	32
12	TRIP1	TRIP2	31
29	SKIPSEL		
4	EN_LDO	VREF2	1
20	V5DRV1	PGOOD1	13
2	TONSEL	PGOOD2	28
	THRM_PAD	GND	PGND
	33	21	22

P5VLTS3_BOOT
P5VLTS3_UGATE
P5VLTS3_PHASE
P5VLTS3_LGATE
(=P5VLTS3_EN)
P5VLTS3_FB
P5VLTS3_ILIM
(=P5VLTS3_EN)
PP5V_S0_MCPREG_VCC
MCPCORES0_REFIN
MCPCORES0_ILIM
PP2V_S0_MCPREG_REF VOLTAGE=2V
Max load 50uA
GND_MCPREG_SGND MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0V

R7570 48.7K 0.1% 1/10W MF 402 <Ra>
R7571 54.9K 0.1% 1/10W MF 402 <Rb>
R7580 475K 0.1% 1/10W MF 402 <Rc> MCP_VID0_L
R7581 237K 0.1% 1/10W MF 402 <Rd> MCP_VID1_L
R7582 110K 0.1% 1/10W MF 402 <Re> MCP_VID2_L

Vout = 0.7V * (1 + Ra / Rb)
Vout = 2.0V * Req / (Ra + Req)
Req = Rb || Rc || Rd || Re

64 IN =P5VLTS3_EN
64 OUT MCPCORES0_PGOOD
64 OUT P5V_LT_S3_PGOOD
64 IN =MCPCORES0_EN

21 IN MCP_VID<0>
21 IN MCP_VID<1>
21 IN MCP_VID<2>

R7590 7.5K 5% 1/10W MF-LF 402
R7591 7.5K 5% 1/10W MF-LF 402
R7592 7.5K 5% 1/10W MF-LF 402
MCP_VID0_RC
MCP_VID1_RC
MCP_VID2_RC
C7590 0.1UF 20% 10V CERM 402
C7591 0.1UF 20% 10V CERM 402
C7592 0.1UF 20% 10V CERM 402

=PPVIN_S0_MCPCORES0
CRITICAL C7560 33UF 20% 16V POLY-TANT CASED2E-SM
C7561 1UF 10% 25V X5R 603-1
C7562 0.001UF 20% 50V CERM 402
CRITICAL Q7560 RJK0305DPB LFPAK-HF
(MCPCORES0_UGATE) MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM GATE_NODE=TRUE
C7564 0.22UF 5% 10V CERM-X7R 603
CRITICAL L7500 1.0UH-13A-5.6M-OHM SM-IHLP-1
=PPMCPCORE_S0_REG
(MCPCORES0_PHASE) MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM SWITCH_NODE=TRUE
(MCPCORES0_LGATE) MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM GATE_NODE=TRUE
CRITICAL Q7565 RJK0328DPB LFPAK-HF
NO STUFF R7596 2.2 5% 1/10W MF-LF 402 EMI request
MCPCORES0_PHASE_SNUBBER
NO STUFF C7596 100PF 5% 50V CERM 402 EMI request
C7567 10UF 20% 6V X5R 603
C7570 0.001UF 20% 50V CERM 402
C7566 10UF 20% 4V X5R 603
CRITICAL C7565 330UF 20% 2.5V POLY-TANT CASE-C2-SM
C7569 0.0027UF 10% 50V CERM 402

Q7580 SSM6N15FEAPE SOT563
Q7582 SSM3K15FV SOD-VESM-HF
PLACE C7565 AND C7568 ONE CLOSE TO U7500 AND ANOTHER CLOSE TO MCP.
=PPVCORE_S0_MCP 8 22 24 46
CRITICAL C7568 330UF 20% 2.5V POLY-TANT CASE-C2-SM
C7568 NEEDS TO BE PLACE CLOSE TO LOAD SIDE CONNECTING IT TO AFTER SENSE RESISTOR INSTEAD OF BEFORE

Vout = See below
MAX CURRENT : 11A
FREQ = 300 KHZ

Rev A01 Production

VID<2:0>	Voltage	Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

M97 DIFFERENCES FROM LAST SYNC ON 12/05/07 TO T18 MLB:
Added C7568 bulk cap on output.
Tied TON to REF.
Changed Q7510 to 376S0674.
C7500 changed to 138S0638.
L7560 changed from T18 MLB inductor to 152S0782.
Changed Q7565 to 376S0637.
Changed R7514 to 280K, R7564 to 180K.

MCP VCORE REGULATOR
SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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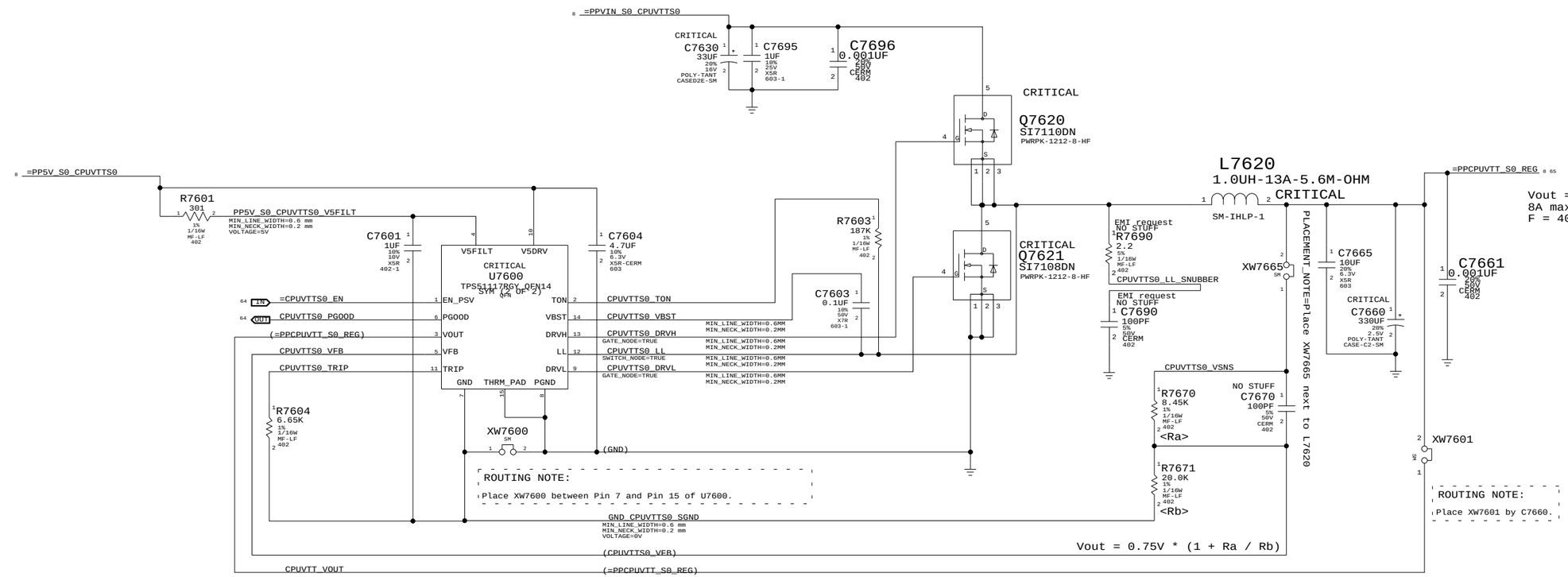
CPUVTT POWER SUPPLY



CPU VTT(1.05V) SUPPLY

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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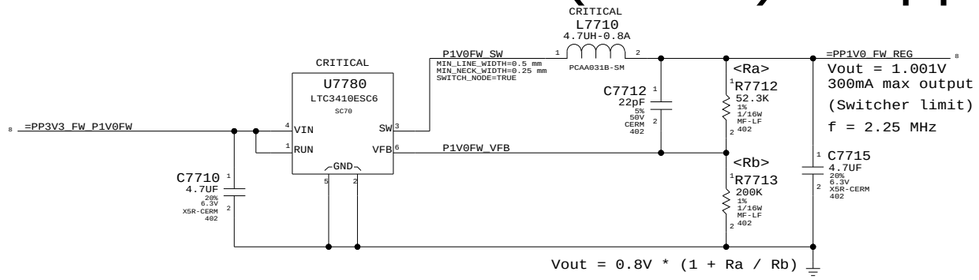
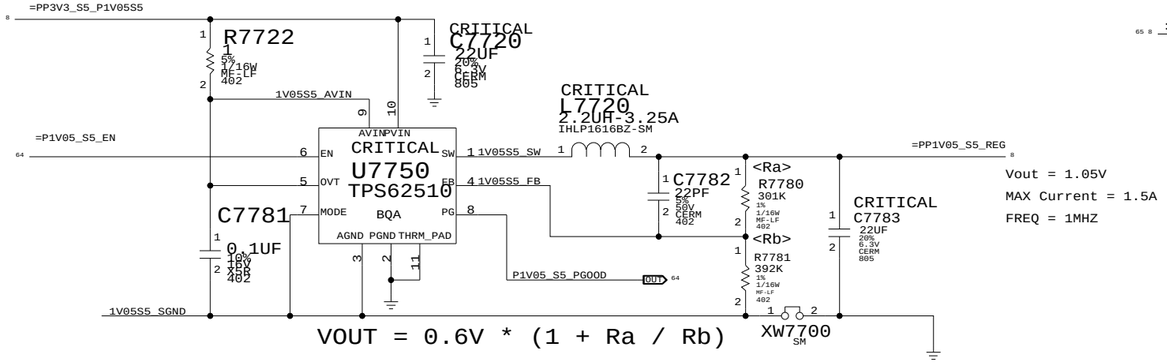
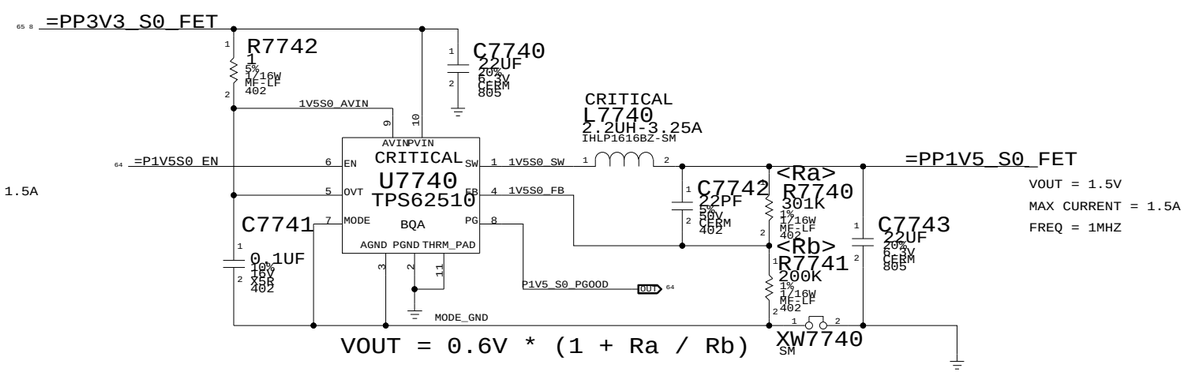
FireWire 1.0V (Core) Supply



MCP 1.05V_S5 AUXC SUPPLY



1.5V S0 SWITCH



MISC POWER SUPPLIES

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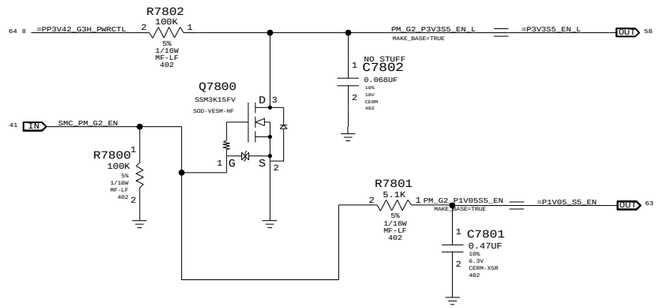
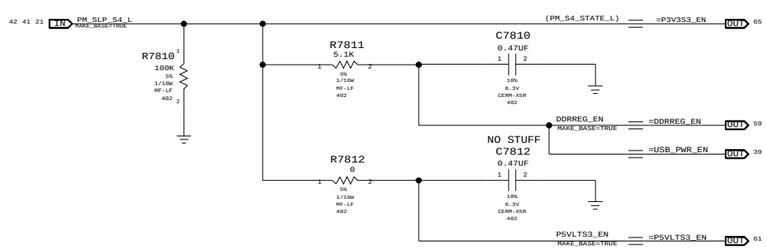
3.3V 1.05V S5 ENABLE

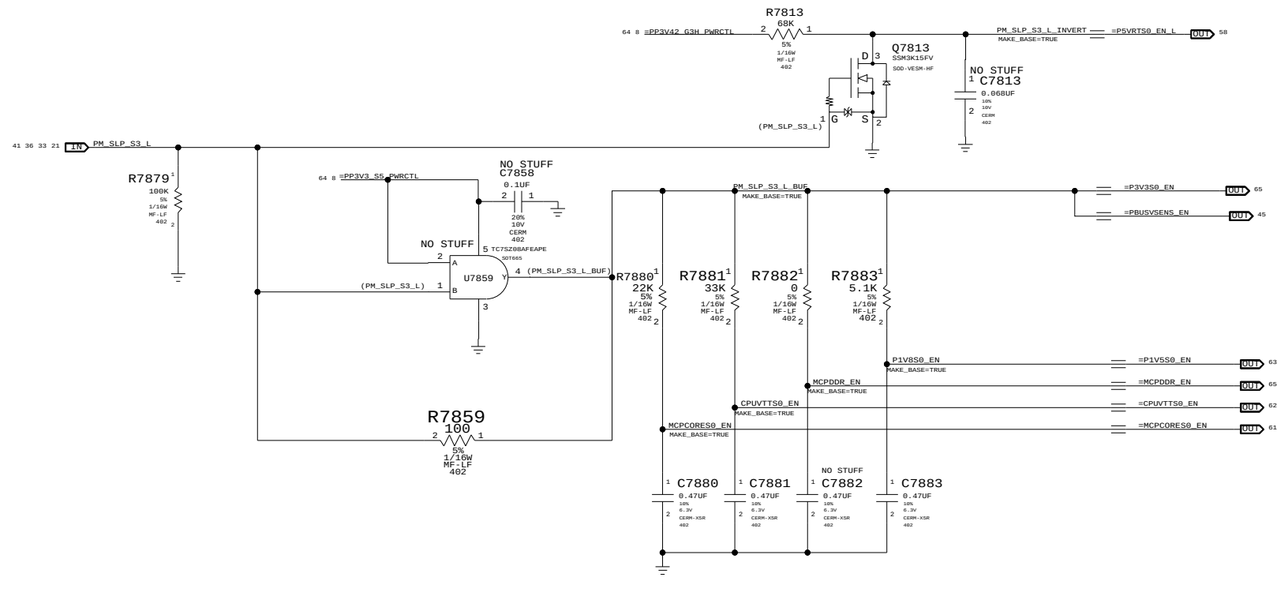


S3 ENABLE



Power Control Signals

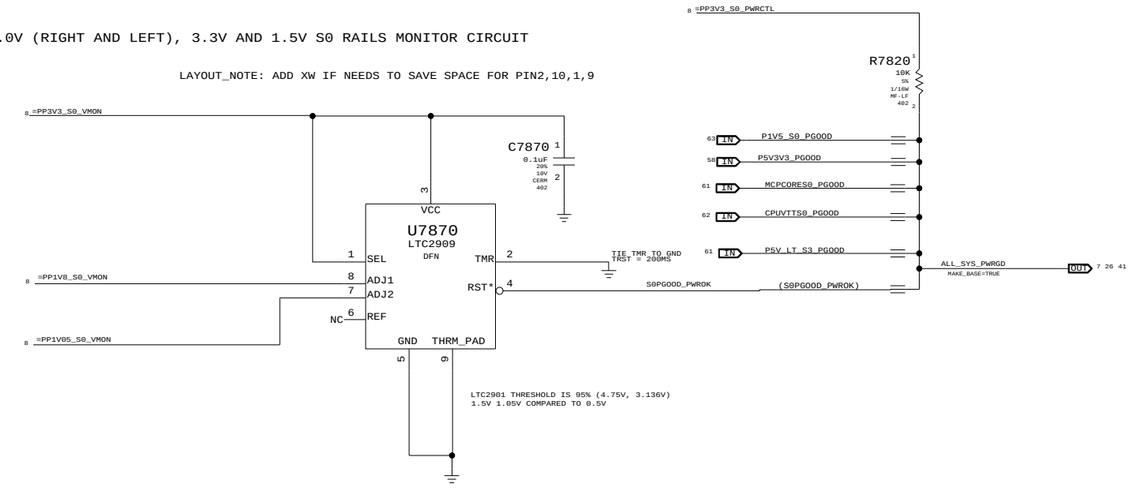
5VLT_S0, 3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE

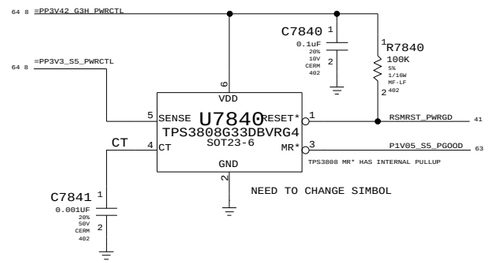


OTHER S0 RAILS PGOOD

5.0V (RIGHT AND LEFT), 3.3V AND 1.5V S0 RAILS MONITOR CIRCUIT

LAYOUT_NOTE: ADD XW IF NEEDS TO SAVE SPACE FOR PIN2,10,1,9





Unused PGOOD signal

POWER SEQUENCING

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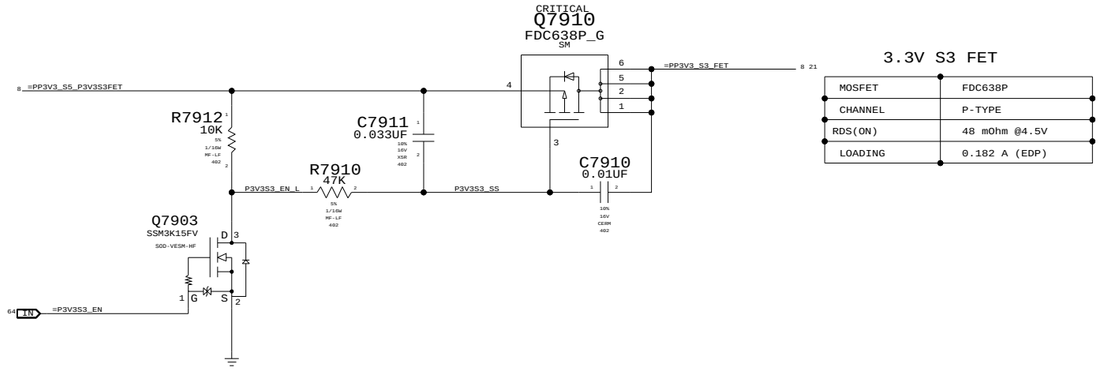
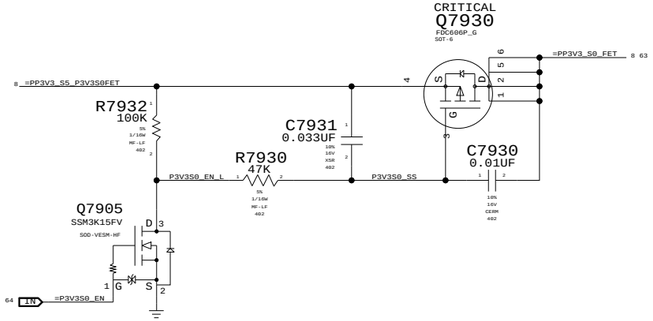
3.3V S3 FET

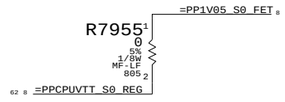


3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET

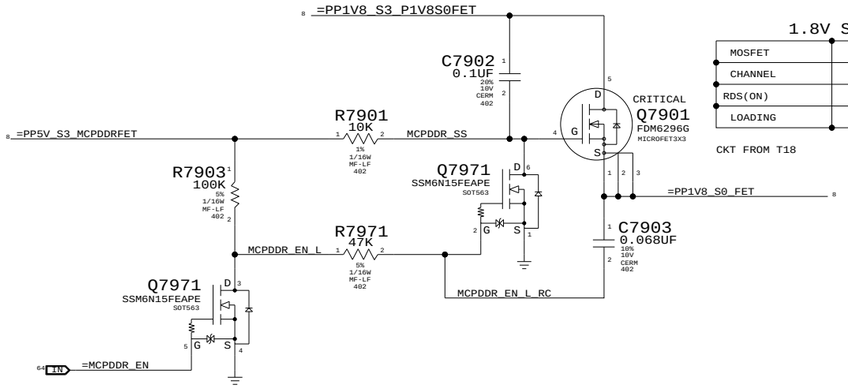


3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)



1.8V S0 FET

(1.8V S0 FET FOR DDR2 MEM)

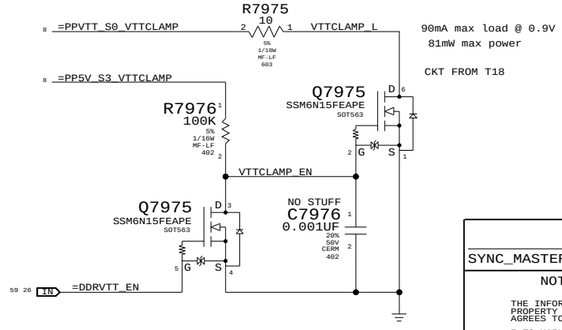


1.8V S0 FET	
MOSFET	FDM6296G
CHANNEL	N-TYPE
RDS(ON)	15 MOHM @4.5V VGS
LOADING	5A (EDP)

CKT FROM T18

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



POWER FETS

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INVERTER CONNECTOR

LCD + CAMERA CONNECTOR

=PP5V_S0_LCD
R9000 100K 1% 1/16W MF-LF 402
INV_PWREN_F_L
R9001 100K 1% 1/16W MF-LF 402
INV_PWREN_L
Q9006 SSM3K15FV SOD-VESM-HF
LVDS_IG_BKL_ON
Q9005 NTK3142PXXH SOT723-3-HF
PP5V_INV
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
C9014 0.0022UF 10% 50V CERM 402
=PPBUS_S5_INV
L9003 FERR-120-OHM-1.5A 0402-LF
PPBUS_ALL_INV_CONN
VOLTAGE=12.6V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
L9002 0 5% 1/10W MF-LF 402
L9000 120-OHM-0.3A-EMI 0402-LF
PP5V_INV_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
L9001 120-OHM-0.3A-EMI 0402-LF
C9001 100PF 5% 50V CERM 402
C9002 100PF 5% 50V CERM 402
C9003 0 5% 1/16W MF-LF 402
C9000 100PF 5% 50V CERM 402
CRITICAL
J9000 78171-0004 M-RT-SM
518S0521
INV_GND
INV_BKLIGHT_PWM
INVT_CHGND
THIS GND CONECTS TO CHASSIS GND
=PP3V3_S0_LCD
BKLT_PLT_RST_L
LVDS_IG_BKL_PWM
CRITICAL
U9053 TC7SZ08AFEAPE SOT665
BKLIGHT_CTL
C9059 0.1UF 10% 16V X5R 402
CRITICAL
Q9003 FDC606P_G SOT-6
=PP3V3_S5_LCD
R9002 100K 5% 1/16W MF-LF 402
R9023 10K 1% 1/16W MF-LF 402
LCDVDD_PWREN_L
LCDVDD_PWREN_L_R
Q9004 SSM3K15FV SOD-VESM-HF
LVDS_IG_PANEL_PWR
PP3V3_LCDVDD_SW
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.30 MM
C9011 0.1UF 10% 16V X5R 402
C9012 10UF 20% 6.3V X5R 603
C9013 0.0033UF 10% 50V CERM 402
L9004 FERR-120-OHM-1.5A 0402-LF
PP3V3_LCDVDD_SW_F
VOLTAGE=3.3V MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM
L9008 120-OHM-0.3A-EMI 0402-LF
=PP3V3_S0_LCD
PP3V3_S0_LCD_F
VOLTAGE=3.3V MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
(LVDS DDC POWER)
IT IS CO-LAY FUNCTION
LVDS_IG_DDC_CLK
LVDS_IG_DDC_DATA
CRITICAL
L9006 90-OHM-200MA AMC2012-SM
LVDS_IG_A_CLK_N
LVDS_IG_A_CLK_P
LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<0>
LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<1>
LVDS_IG_A_DATA_N<2>
LVDS_IG_A_DATA_P<2>
LVDS_IG_A_CLK_F_N
LVDS_IG_A_CLK_F_P
CRITICAL
L9007 90-OHM-200MA
USB_CAMERA_P
USB_CAMERA_N
L9005 FERR-120-OHM-1.5A AMC2012-SM
=PP5V_S3_CAMERA
PP5V_S3_CAMERA_F
VOLTAGE=5V
MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.30 MM
C9016 0.001UF 10% 50V CERM 402
C9015 0.001UF 10% 50V CERM 402
C9010 0.001UF 10% 50V CERM 402
USB2_CAMERA_CONN_P
USB2_CAMERA_CONN_N
CRITICAL
J9001 S-050162B F-RT-SM
=GND_CHASSIS_LVDS
LCD I/F
CAMERA I/F
Plexi: 516S0212
*Enclosure: 518S0364
=PP3V3_S0_LCD
R9015 2.7K 5% 1/16W MF-LF 402
R9016 2.7K 5% 1/16W MF-LF 402
LVDS_IG_DDC_CLK
LVDS_IG_DDC_DATA
LVDS_IG_BKL_PWM
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
R9019 1K 5% 1/10W MF-LF 402
R9018 1K 5% 1/16W MF-LF 402
R9012 1K 5% 1/10W MF-LF 402

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

INVERTER,LVDS

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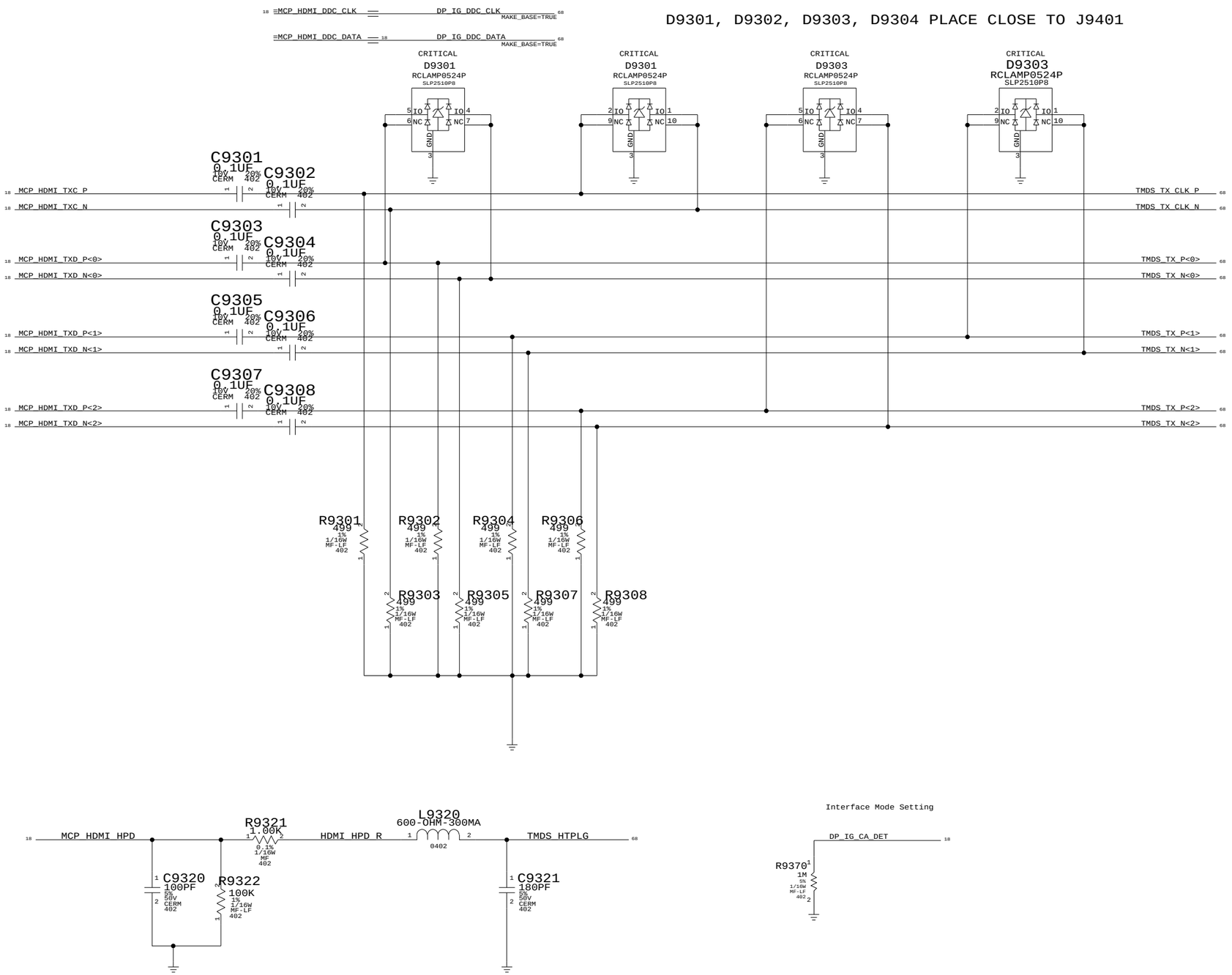

TMDS ALIASES

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Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

TMDS(MINI DVI) INTERFACE

=PP5V_S0_TMDS — VOLTAGE=5V, MIN_LINE_WIDTH=0.30 MM, MIN_NECK_WIDTH=0.20 MM

C9408 0.047UF 10% 10V X7R 402 — C9408 PLACE CLOSE TO F9404

C9409 0.047UF 10% 10V X7R 402 — C9409 PLACE CLOSE TO Z0912

CRITICAL F9404 0.5AMP-13.2V SM-HF

PP5V_S0_TMDS_FUSE — VOLTAGE=5V, MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM

NEED CHANGE SYMBOL

D9401 1SS418 SOD-723-HF

L9444 600-OHM-300MA 0402

PP5V_S0_DVIPORT — VOLTAGE=5V, MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM

C9404 0.1UF 20% 16V CERM 402

=GND_CHASSIS_TMDS_UPPER

DVI power DIODE on page 95 (D9500)

PP5V_S0_DVIPORT_D

R9462 2.7K 5% 1/16W MF-LF 402

R9463 2.7K 5% 1/16W MF-LF 402

TMDS_HTPLG

=PP3V3_S0_TMDS

R9421 2.7K 5% 1/16W MF-LF 402

R9422 2.7K 5% 1/16W MF-LF 402

Q9401 SSM6N15FEAPE SOT563

DP_IG_DDC_CLK

DP_IG_DDC_DATA

NOTE: CRT_DDC_* ARE NOT 5V COMPLIANT

GPU_CRT_DDC_CLK

GPU_CRT_DDC_DATA

Q9401 SSM6N15FEAPE SOT563

C9410 0.001UF 10% 50V CERM 402

C9411 220PF 5% 25V CERM 402

C9412 220PF 5% 25V CERM 402

CRITICAL D9400 SC70-6-1 RCLAMP0504F

PLACE THE RESISTOR CLOSE TO MCP79 AND THE CAP NEAR J9401

=PP3V3_S0_TMDS

C9460 0.1UF 20% 16V CERM 402

CRITICAL U9404 SN74LVC2G125DCU

CRT_IG_HSYNC — R9460 0 5% 1/16W MF-LF 402 — CRT_HSYNC_LS_R — 125 — CRT_HSYNC_LS — R9470 39 5% 1/16W MF-LF 402 — VGA_HSYNC

NO STUFF C9442 47PF 5% 50V CERM 402

PLACE THE RESISTOR CLOSE TO MCP79 AND THE CAP NEAR THE CONNECTOR

CRITICAL U9404 SN74LVC2G125DCU

CRT_IG_VSYNC — R9461 0 5% 1/16W MF-LF 402 — CRT_VSYNC_LS_R — 125 — CRT_VSYNC_LS — R9471 39 5% 1/16W MF-LF 402 — VGA_VSYNC

NO STUFF C9443 47PF 5% 50V CERM 402

OMIT

CRITICAL J9401 MINI-DVI-M42-MG3 F-RT-TH-HF

PP5V_S0_DVIPORT

NC NC

VGA_B VGA_HSYNC VGA_G VGA_VSYNC VGA_R

TMDS_TX_CONN_P<2> TMDS_TX_CONN_N<2> TMDS_TX_CONN_P<1> TMDS_TX_CONN_N<1> TMDS_TX_CONN_P<0> TMDS_TX_CONN_N<0> TMDS_TX_CONN_CLK_P TMDS_TX_CONN_CLK_N

=GND_CHASSIS_TMDS_UPPER =GND_CHASSIS_TMDS_DOWN

CRITICAL L9405 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<2> TMDS_TX_N<2>

CRITICAL L9407 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<1> TMDS_TX_N<1>

CRITICAL L9406 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<0> TMDS_TX_N<0>

CRITICAL L9404 300-OHM-100MA 1210-4SM1 — TMDS_TX_CLK_P TMDS_TX_CLK_N

for VG signal trace, we need follow NV's recommendation. So we need change the segment impedance base on NV design guide.
for A segment: 37.5 ohm from MCP to 150 ohm PD res: Top/bottom layer width is 0.18 mm
for B segment: 50 ohm B/W 2 150 PF res. inner layer width is 0.09 mm top/bottom layer width is 0.115 mm
for C segment: 75 ohm from FL to connector, top/bottom layer width is 0.076 mm.

CRT_IG_R_C_PR — R9493 150 1% 1/10W MF-LF 402

CRT_IG_G_Y_Y — R9494 150 1% 1/10W MF-LF 402

CRT_IG_B_COMP_PB — R9495 150 1% 1/10W MF-LF 402

R9493, R9494, R9495 PLACE CLOSE TO U1400

CRITICAL FL9400 210MHZ MEA2010P-SM

R9490 150 1% 1/10W MF-LF 402

R9491 150 1% 1/10W MF-LF 402

R9492 150 1% 1/10W MF-LF 402

R9490, R9491, R9492 PLACE CLOSE TO FL9400

MINI-DVI CONNECTOR

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 42 60
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 42
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_EFOM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	10 14 60
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	7 13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	7 13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 60
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	60
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 27
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 7 10 13
	XDP_TDO1	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 7 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 7 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 7 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	7 10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	7 10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	7 13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	11 60
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 60
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 60
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

CPU/FSB Constraints

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SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 100 OF 109	

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 28 30
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 28 30
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 28 30
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 29 30
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 29 30
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 29 30
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

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D	051-8089	02

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7 31
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7 31
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 31
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 31
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7 17 31
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7 17 31
	PCIE_90D	PCIE	PCIE_FW_R2D_P	35
	PCIE_90D	PCIE	PCIE_FW_R2D_N	35
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 35
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 35
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	35
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	9 17
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	9 17
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	9 17
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	9 17
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9 17
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9 17
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	7 17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	7 17 31
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 35
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 35
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	9 17
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	9 17
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
CRT_RED	CRT_MCP_P	CRT	CRT_IG_R_C_PR	18 68
CRT_GREEN	CRT_MCP_P	CRT	CRT_IG_G_Y_Y	18 68
CRT_BLUE	CRT_MCP_P	CRT	CRT_IG_B_COMP_PB	18 68
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	18 68
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	18 68
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	9 18
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	9 18
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	
DP_AUX_CH	DP_100D	DISPLAYPORT	TP_DP_IG_AUX_CH_P	
DP_AUX_CH	DP_100D	DISPLAYPORT	TP_DP_IG_AUX_CH_N	
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 25
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 25
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 66
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 66
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	7 18 66
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	7 18 66
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 25
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 25
SATA_HDD_R2D	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_P	20 38
	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_N	20 38
	SATA_100D_HDD	SATA	SATA_HDD_R2D_P	7 38
	SATA_100D_HDD	SATA	SATA_HDD_R2D_N	7 38
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_P	38
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_N	38
SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA_HDD_D2R_P	20 38
	SATA_100D_HDD	SATA	SATA_HDD_D2R_N	20 38
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_P	7 38
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_N	7 38
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_ODD_R2D_P	38
	SATA_100D	SATA	SATA_ODD_R2D_N	38
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	7 38
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	7 38
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 38
	SATA_100D	SATA	SATA_ODD_D2R_N	20 38
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 38
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	38
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	38
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

MCP Constraints 1

SYNC_MASTER=K36B_MLB SYNC_DATE=08/17/2008

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SCALE	SHT	OF
NONE	102	109

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0> 7 13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L 19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0> 7 19 41 43
LPC_FRAME_L0	LPC_55S	LPC	LPC_FRAME_L 7 19 41 43
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 19 26
MCP_LPC_CLK	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 19 26
MCP_LPC_CLK	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 26 41
MCP_LPC_CLK	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 7 26 43
USB_EXTA	USB_90D	USB	USB_EXTA_P 20 39
USB_EXTA	USB_90D	USB	USB_EXTA_N 20 39
USB_EXTA	USB_90D	USB	USB2_EXTA_MUXED_P 39
USB_EXTA	USB_90D	USB	USB2_EXTA_MUXED_N 39
USB_EXTA	USB_90D	USB	USB2_EXTA_F_P 39
USB_EXTA	USB_90D	USB	USB2_EXTA_F_N 39
USB_MINI	USB_90D	USB	USB_MINI_P 9 20
USB_MINI	USB_90D	USB	USB_MINI_N 9 20
USB_MINI	USB_90D	USB	USB2_AIRPORT_P 7 31
USB_MINI	USB_90D	USB	USB2_AIRPORT_N 7 31
USB_EXTD	USB_90D	USB	USB_EXTD_P 9 20
	USB_90D	USB	USB_EXTD_N 9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 20 66
USB_CAMERA	USB_90D	USB	USB_CAMERA_N 20 66
USB_CAMERA	USB_90D	USB	USB2_CAMERA_CONN_P 7 66
USB_CAMERA	USB_90D	USB	USB2_CAMERA_CONN_N 7 66
USB_IR	USB_90D	USB	USB_IR_P 20 40
USB_IR	USB_90D	USB	USB_IR_N 20 40
USB_TPAD	USB_90D	USB	USB_TPAD_P 9 20
USB_TPAD	USB_90D	USB	USB_TPAD_N 9 20
USB_TPAD	USB_90D	USB	CONN_TPAD_USB_P 7 49
USB_TPAD	USB_90D	USB	CONN_TPAD_USB_N 7 49
USB_BT	USB_90D	USB	USB_BT_P 9 20
USB_BT	USB_90D	USB	USB_BT_N 9 20
USB_BT	USB_90D	USB	USB2_BT_F_P_CONN 7 40
USB_BT	USB_90D	USB	USB2_BT_F_N_CONN 7 40
USB_EXTB	USB_90D	USB	USB_EXTB_P 20 39
USB_EXTB	USB_90D	USB	USB_EXTB_N 20 39
USB_EXTB	USB_90D	USB	USB2_EXTB_F_P 39
USB_EXTB	USB_90D	USB	USB2_EXTB_F_N 39
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 9 20
	USB_90D	USB	USB_EXCARD_N 9 20
USB_EXTC	USB_90D	USB	USB_EXTC_P 9 20
	USB_90D	USB	USB_EXTC_N 9 20
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK 7 13 21 44
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA 7 13 21 44
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK 21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA 21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 21 52
	HDA_55S	HDA	HDA_BIT_CLK_R 21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 21 52
	HDA_55S	HDA	HDA_SYNC_R 21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L 21
	HDA_55S	HDA	HDA_RST_L 21 52
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 21 52
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 21 52
	HDA_55S	HDA	HDA_SDOUT_R 21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R 21 26
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 26 41
SPI_CLK	SPI_55S	SPI	SPI_CLK_R 21 43
	SPI_55S	SPI	SPI_CLK_MUX 43 51
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 21 43
	SPI_55S	SPI	SPI_MOSI_MUX 43 51
SPI_MISO	SPI_55S	SPI	SPI_MISO_MUX 43 51
	SPI_55S	SPI	SPI_MISO_R 51
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 21 43
	SPI_55S	SPI	SPI_CS0_L

MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 33
	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0	
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 32
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 32
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	32
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 32
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	32
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 32
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	32 34
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	32 34

Ethernet Constraints

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	35 37
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_PORT_A_P	37
FW_P1_TPA	FW_110D	FW_TP	FW_PORT_A_N	37
FW_P1_TPB	FW_110D	FW_TP	FW_PORT_B_P	37
FW_P1_TPB	FW_110D	FW_TP	FW_PORT_B_N	37

Port 2 Not Used

FireWire Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S5	SMB	SMBUS_SMC_A_S3_SCL	44
SMBUS_SMC_A_S3_SDA	SMB_5S5	SMB	SMBUS_SMC_A_S3_SDA	44
SMBUS_SMC_B_S0_SCL	SMB_5S5	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_5S5	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_5S5	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_5S5	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_5S5	SMB	SMBUS_SMC_BSA_SCL	44
SMBUS_SMC_BSA_SDA	SMB_5S5	SMB	SMBUS_SMC_BSA_SDA	44
SMBUS_SMC_MGMT_SCL	SMB_5S5	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_5S5	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

SMC Constraints

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K36B BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	*	Y	0.145 MM	0.145 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.275 MM	0.275 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.109 MM	0.109 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.089 MM	0.089 MM		0.230 MM	0.230 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.152 MM	?
3X_DIELECTRIC	-	0.228 MM	?
4X_DIELECTRIC	-	0.304 MM	?
5X_DIELECTRIC	-	0.380 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

K36B RULE DEFINITIONS

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